CMOS-BASED AMPLITUDE AND PHASE CONTROL CIRCUITS DESIGNED FOR MULTI-STANDARD WIRELESS COMMUNICATION SYSTEMS

A Dissertation

Presented to

The Academic Faculty

by

Yan-Yu Huang

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2011

CMOS-BASED AMPLITUDE AND PHASE CONTROL CIRCUITS DESIGNED FOR MULTI-STANDARD WIRELESS COMMUNICATION SYSTEMS

Approved by:

Dr. J. Stevenson Kenney, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Thomas G. Habetler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Kevin T. Kornegay
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Paul A. Kohl
School of Chemical and Biomolecular Engineering
Georgia Institute of Technology

Dr. Chang-Ho Lee
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: June 29, 2011

ACKNOWLEDGEMENTS

I would like to express my gratitude to my advisor, Professor James Stevenson Kenney, for his excellent guidance and all the suggestions that help me conduct the research, solve the problems, and improve my dissertation. I would also like to thank my committee members: Professor Kevin T. Kornegay, Professor Thomas G. Habetler, Professor Paul A. Kohl, and Dr. Chang-Ho Lee for their time in reviewing my dissertation and all the invaluable suggestions.

I would also like to express my appreciation to the leaders in various projects I was involved during the past four years, Dr. Joy Laskar, Dr. Chang-Ho Lee, and Dr. Wangmyoong Woo. Their valuable comments on my work and relative knowledge about the project have been a tremendous help to me. All the experiences I gained and the lessons I learned from the projects and from them have been my best tools for dealing with the problems encountered when writing this dissertation.

This work will not have been completed without the assistance and insightful feedback from my previous and present senior colleagues, Dr. Dong-Ho Lee, Dr. Kyu Hwan An, Dr. Ockgoo Lee, Dr. Youngchang Yoon, Dr. Jihwan Kim, Dr. Joonhoi Hur, Kun-Seok Lee, Kwanyeob Chae, Dr. Hyungwook Kim, Hamhee Jeon, Hyungwoon Kim, Taejin Kim, Dr. Eungjung Kim, Dr. Jeongwon Cha, and Dr. Yunseo Park, in Microwave Application Group (MAG). The supports from other MAG members, Michael Oakley, David Yeh, Shih-Chie Shin, and Sen-Wen Hsiao, are also critical for me to finish my dissertation. I would also like to appreciate my supervisor in Broadcom, Dr. Fei-Ran Yan, and other colleagues. All the knowledge I learned there as an intern has greatly improved my skills in doing experiments. I also wish to thank DeeDee Bennett, and Angelika Braig, I would have been unable to concentrate on my research without their continuous support.

I would also like to take this chance to express my gratitude and apology to my friends in TSRB, John Poh and Kevin Chuang. They did me a lot of favors during the past four years, especially when I was away from the school doing internship.

Most of all, I owe the deepest gratitude to my parents. Their unconditional love and supports encourage me to pursue my dreams and to overcome all the difficulties during the past four years.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

2G	second generation
3G	third generation
A/D	analog-to-digital
AC	alternating current
ACPR	adjacent channel power ratio
AGC	automatic gain control
AM-AM	amplitude modulation
AMED	amplitude modulation error detector
BER	bit error rate
BJT	bipolar junction transistor
CMOS	complementary metal-oxide semiconductor
COB	circuit-on-board
CS	common-source
CG	common-gate
DC	direct current
DIBL	drain induced barrier lowering
EDGE	enhanced data rates for global system for mobile communications evolution
EER	envelope elimination and restoration
EVM	error vector magnitude
F	noise factor
FTPS	forward type phase shifter
GIDL	gate induce drain leakage
g_m	transconductance
GMSK	gaussian minimum-shift keying
GSM	global system for mobile communications
HPSK	hybrid phase shift keying
I	in-phase
IIP_3	input referred third-order intercept point
IL	insertion loss
IP_{1dB}	input referred 1-dB gain compression point
LO	local oscillation
LC	inductor and capacitor
LPF	low-pass filter
MOSFET	metal-oxid-semiconductor field-effect transistor
NF	noise figure
NMOS	n-channel metal-oxid-semiconductor field-effect transistor

OIP_3	output referred third-order intercept point
OP_{1dB}	output referred 1-dB gain compression point
OP-AMP	operational amplifier
P_{1dB}	1-dB gain compression point
PA	power amplifier
PAE	power-added efficiency
PAPR	peak-to-average power ratio
PCB	printed circuit board
PLL	phase-lock loop
PMED	phase modulation error detector
PPF	poly-phase filter
PSK	phase shift keying
Q	quadrature-phase
RC	resistor and capacitor
RF	radio frequency
RTPS	reflection-type phase shifter
VGA	variable-gain amplifier
VPS	variable-phase shifter
V_{TH}	threshold voltage
VVA	voltage-controlled variable attenuator
WCDMA	wideband code division multiple access

SUMMARY

The growing demands for accessing multimedia contents through wireless handsets have accelerate the migration to more advanced communication standards that can exchange data at a higher rate. However, the complicated symbol constellations of the advanced modulation schemes used by those high-speed standards bring new challenges to the RF frontend design. The strict linearity requirement for transmitters, especially for power amplifiers (PAs), is extremely difficult to meet unless they are designed with high performance and much expensive technologies. The objective of this research is to design wideband linearization circuits in complementary metal-oxide semiconductor (CMOS), a less expensive technology, for an analog-predistorted PA system. These circuits are responsible for canceling out the non-linearity, namely, amplitude and phase distortion, of a PA.

The dissertation first proposes a highly linear wideband variable attenuator for applications require amplitude-distortion compensation at a very high signal power. The attenuator utilizes an adaptive bias circuit in conjunction with other linearization techniques to enhance its gain flatness. With the suggested techniques, the attenuator successfully demonstrates its ability for controlling the amplitude of a high-power signal. For those applications take a smaller input power but require gain for the non-linear amplitude compensation, the dissertation also presents a linear variable gain amplifier (VGA) topology which is suitable for the role. To provide linear-in-dB tuning and linearity at the same time, the VGA uses a highly linear variable attenuator with an adaptively biased fixed-gain stage. Different from the conventional attenuator-based VGAs, the high linearity of the suggested attenuator topology allows it to be put after the gain stage in the presented VGA design. This arrangement not only gives the VGA a better linearity

and maintains its noise performance at the same time, but also a flat gain response even at a higher input power.

The dissertation also proposes a very compact, linear-in-degree tuned variable phase shifter (VPS) as the phase predistorter in the PA system. This design uses a novel poly-phase filter topology to produce a set of an orthogonal phase vector. A specially designed control circuit combines these vectors and generates an output signal with different phases, while having very small gain mismatches at different phase setting. All the mentioned designed are implemented in a commercial-available 0.18-μm CMOS technology, and the performances are verified through measurements.

To validate the functionally of the presented amplitude and phase predistorters in an analog-predistorted PA system, a system level simulation is performed in the end of this dissertation. The presented gain and phase control circuits are put together with the gain and phase detection circuits, which are built based on the same CMOS technology model. The whole analog predistortion system considerably suppresses the gain and phase variation of a non-linear PA, significantly improves the linearity performance of the overall PA system.

CHAPTER 1
INTRODUCTION

1.1 MOTIVATION

Twenty years after the first commercial launch of the second-generation generation (2G) mobile communication systems, a rapid growth of the smartphone market in recent years has demonstrated users' strong demands for mobile services in addition to voice communication. These services, for example, accessing to the Internet, using navigation, and video streaming, are likely to transfer data at a higher rate than voice communication. The requirements on the data exchange rate therefore are far exceeding the maximum speed of 2G standards, such as Global Systems for Mobile communications (GSM), can provide. To boost the data rate within an already-crowded RF spectrum, the tendency of recent transmitter frontend designs is to integrate multi-standard communication systems into a single chip, providing both new, upcoming technology and keeping compatibility with lapsing standards at the same time [1], [61]. As demonstrated Figure 1.1, the expected market share of mobile handsets that support a wide-band code division (WCDMA), a third-generation (3G) standard, will soon be larger than handsets that supports 2G standards only.

However, theses advanced modulation schemes usually involve phase and amplitude modulations, thereby requiring a linear RF frontend to transmit/receive signals without distorting them. Table 1.1 lists several popular 2G and 3G standards, their corresponding modulation

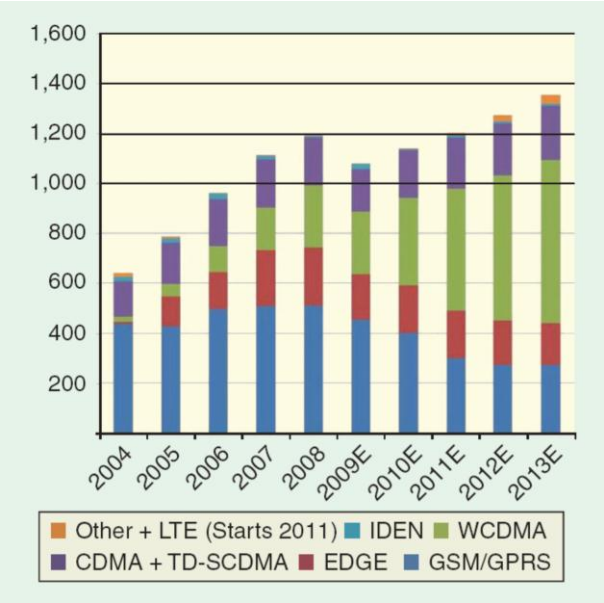


Figure 1.1 Cell phone handset unit growth year over year forecast worldwide (in millions) [61]

Table 1.1 Modulation schemes and their characteristics

System	Modulation	Bandwidth	Peak to Average Power Ratio	Peak to Minimum Power Ratio
GSM	GMSK	0.20 MHz	0 dB	0 dB
EDGE	8PSK	0.20 MHz	3.2 dB	17 dB
WCDMA	HPSK	3.84 MHz	3.5-3.7 dB	Infinite

schemes, and the peak-to-average power ratio (PAPR) of each scheme, while Figure 1.2 shows the constellation and signal trajectories of different modulation schemes. Comparing the Gaussian Minimum Shift Keying (GMSK) used by GSM with the π/3 8-Pase Shift Keying (π/3 8-PSK used by enhanced data rate GSM evolution (EDGE), or with the Hybrid Phase Shift Keying (HPSK) used by WCDMA, we could clear see two major differences. The first one is the amount of symbols on the constellation increases from GSM modulation to EDGE/WCDMA

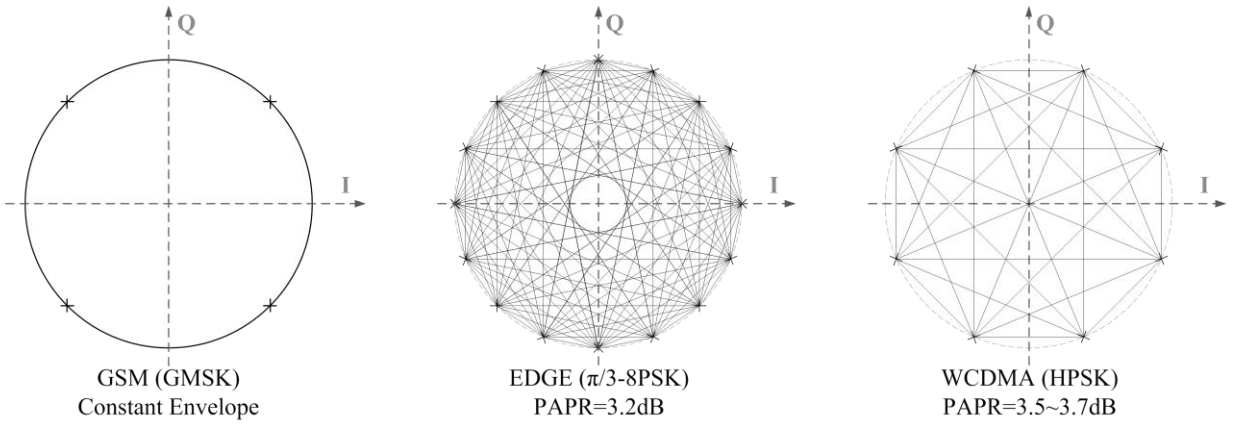


Figure 1.2 The constellation diagram of GSM, EDGE and WCDMA

modulations; and the trajectories from symbol to symbol no longer having constant amplitudes in EDGE/WCDMA modulations. As a consequence, the requirements on the amplitude errors, the phase errors, and the error vector magnitude (EVM) of the latter two modulations will be much strict to achieve the same bit error rate (BER). In other words, the RF front end of an EDGE or WCDMA transceiver should have minimum AM-AM (amplitude modulation) or AM-PM (phase modulation) errors as compared to a GSM transceiver.

Although CMOS is the most promising technology for a multi-standard radio in the mobile handset, its inferior RF performance made designing a linear RF front-end, specially a linear CMOS PA in the transmitter, a great challenge [2]. CMOS technology is well known for its low production-cost, high-integration, and low power-consumption. These are great advantages for implementing multi-standard transceivers with their control circuits and even the baseband logics in to a single chip. However, its lossy silicon substrate, severe parasitic effects, a comparably nonlinear transconductance, as well as a lower break down voltage had once prevented the final integration of the most performance demanding part, PA, into a single chip. Fortunately, with all

the research efforts on various linearization techniques, we have seen the possibility of making CMOS PAs for a linear transceiver.

In several of the proposed solutions for linear PA, phase and amplitude control circuits play essential role in correcting the AM-AM and AM-PM errors. These linear PAs use either voltage controlled variable attenuators (VVA) or variable gain amplifiers (VGA), along with variable phase shifters (VPS) to correct the corresponding errors. These circuits have long been studied and are widely used in different transceiver systems. For example, a VVA or VGA can be found in a homodyne or heterodyne receivers, in charging of controlling the received signal strength going to the baseband circuits. On the other hand, a VPS could be easily found in millimeter applications, such as phase array or beam-forming systems. Nevertheless, a VVA, a VGA or a VPS here in the PA system face a very different operation condition than their counterparts in traditional receivers or millimeter-wave systems. Therefore, it is required to address the special design issues of the gain and the phase control circuits in a linear PA system, and of course to explore new circuit topologies those are most suitable for the specified system.

1.2 NONLINEAR RESPONSES OF PAS

Before dealing with the non-linearity of the PA, it is worth to know where the non-linearity comes from. PAs in almost all the recent mobile products are designed with transistor. Transistors are not linear devices and can only perform linear amplification for a limited input/output voltage range. In a common-source (CS) amplifier, we usually assume that the gain is the transconductance (g_m) of the CS stage multiplies the output impedance. However, the g_m and the output impedance are actually functions of input and output voltage values. These relations will be most obvious when the CS amplifier is operated at high frequency and power. At a higher frequency, the parasitic capacitance starts to dominate the output impedance, while at

a very high voltage swing the value of the parasitic capacitance starts to vary dramatically with the voltage swing. In addition, a very high voltage swing also causes other non-linear effects such as drain-induced barrier lowering (DIBL) and gate-induced drain leakage (GIDL). Therefore, if we plot the gain/phase of an amplifier, specially a PA, we are expected to see a deviation from the original value at a higher input power. As shown in Figure 1.3, these

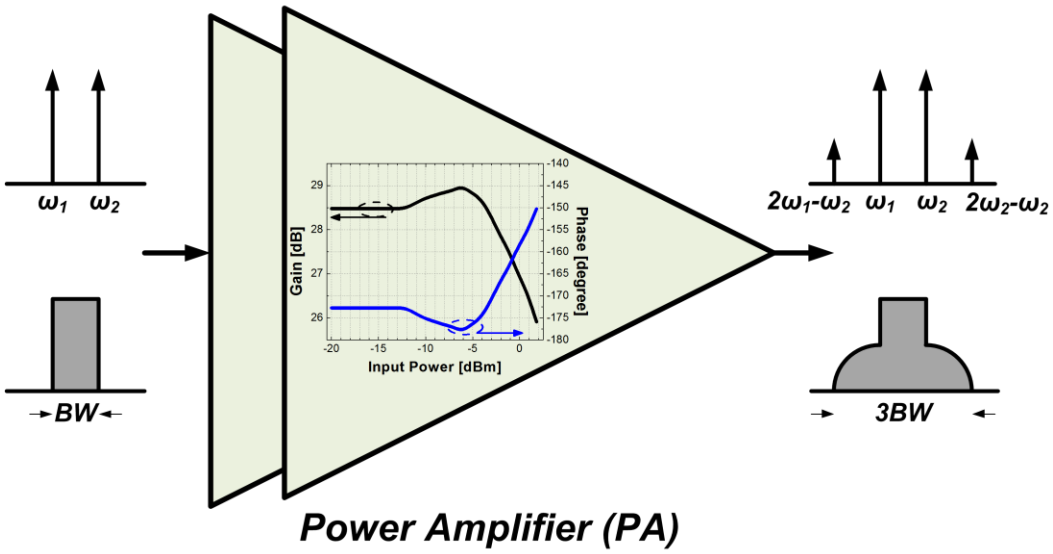


Figure 1.3 Power dependent gain/phase variation, harmonic distortion and spectral regrowth of a PA

variations degrade the performance of a PA. With all the nonlinearity, the transfer characteristics of a PA should not be modeled as a straight line but with a higher order polynomial. Assuming the PA is memoryless for simplicity, we could relate the input and output of a PA by [3]:

$$V_{OUT}(t) \approx a_1 \times V_{IN}(t) + a_2 \times V_{IN}^{\ 2}(t) + a_3 \times V_{IN}^{\ 3}(t) \qquad (1.1).$$

When two signals with different frequencies (ω_1 and ω_2) are applied to the input, for example if

$$V_{IN}(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \qquad (1.2),$$

then the output can be found by calculating:

$$\begin{aligned} V_{OUT}(t) \approx & a_1 \times \left[A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \right] \\ & + a_2 \times \left[A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \right]^2 + a_3 \times \left[A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \right]^3 \end{aligned} \quad (1.3).$$

If ω_1 is close to ω_2, we find that the output will contains frequency components not just at ω_1 and ω_2 but also tones at $2\omega_2$-ω_1 and $2\omega_1$-ω_2 even a very good filter is put at the output. The output terms for these two frequencies can be calculated by organizing (1.3):

$$\begin{cases} 2\omega_1 - \omega_2 : \dfrac{3a_3 A_1^2 A_2}{4} \cos(2\omega_1 - \omega_2) \\ 2\omega_2 - \omega_1 : \dfrac{3a_3 A_1 A_2^2}{4} \cos(2\omega_2 - \omega_1) \end{cases} \quad (1.4).$$

Therefore, two extra components will be spotted on the output spectrum, as plotted in Figure 1.3, and the phenomenon is well-known as the third-order intermodulation distortion. If modulated signals are applied to the PA (which can be viewed as a combination of more tones), it is expected to see an expansion on the output spectrum and is known as spectral regrowth.

Two problems arise with such a non-linear behavior of the PA. The first one is the excessive energy appeared in the nearby spectrum may violate the spectrum mask. The other problem is that AM-AM and AM-PM errors will change the amplitude/phase information of the transmitted symbol, increasing the EVM and the BER. Therefore, linearization techniques are critical for PA performance especially for the one that designed for the advanced communication standards.

1.3 LINEARIZATION TECHNIQUES FOR PAS

PA linearization techniques have long been a popular research topic, and many methods are proposed to resolve the non-linear issues. Although this research work is mainly focused on the most promising technique: adaptive predistortion, introductions to the other methods will help demonstrate the advantages of adaptive predistortion over other techniques.

1.3.1 Feedback

Feedback probably is the first method comes to one's mind to overcome the non-linearity. After all, it was invented to suppress the gain variation of an amplifier. To get a very good linearity and stability, the loop gain of the amplifier has to be very high, and the poles and the zeros should be carefully placed. However, these are extremely difficult tasks for PAs. Their operation frequencies are much higher; the parasitic from various sources such as wire-bonding, pads, and even package are much complicated, posing a great difficulty when dealing with zeros and poles. In addition, PAs are high-gain circuits and hence tend to oscillate even without a feedback. If we add a feedback with high loop gain and directly on the RF path, as shown in Figure 1.4, it is almost guaranteed to see an oscillation from a PA.

There is a way to relieve the oscillation issue. Since the signal fed to the PA is a modulated signal from baseband, it is possible to down-convert the output of the PA first and then feed it back to the baseband of the transmitter. Nevertheless, almost all the 2.5G or 3G communication standards have both I and Q signals. It requires multiple mixers to down-convert the signal properly. This adds too much complexity to the overall PA system, and therefore is not a very attractive solution.

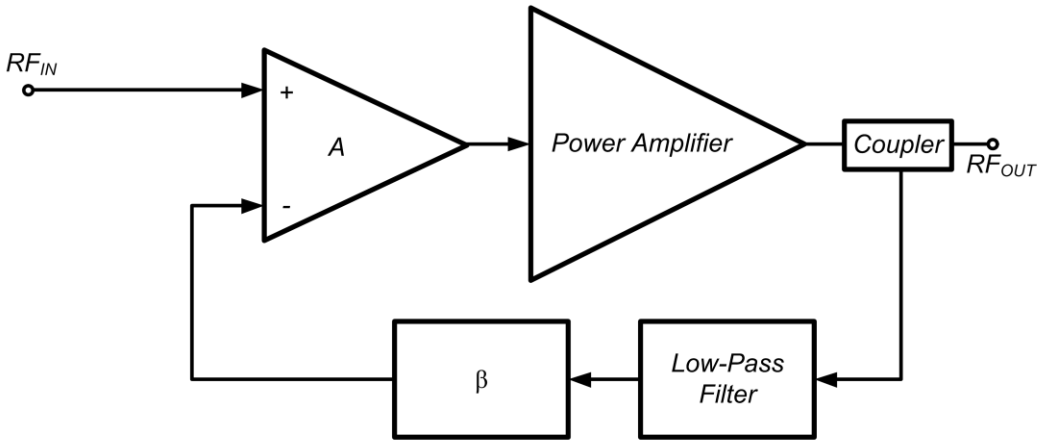


Figure 1.4 The block diagram of a feedback PA system

1.3.2 Feedforward

The advantage of a feedforward PA over a feedback PA is on the stability and gain. Figure 1.5 demonstrated the topology and required building blocks in a feedforward PA. An amplifier measured the distortion between the input and output of the PA, and then feed it to a summing circuit. The output of that summing circuit is therefore the output of a PA deducts its distortion, resulting in a gain characteristic with very low distortion. In addition, the output of a feedforward PA is not a function of the past signals, and there is no close loop for an oscillation to occur. Moreover, unlike feedback, the feedforward topology does not degrade the overall gain of the original amplifier. Therefore, the designers do not need to sacrifice other performances to over-design the gain of the PA.

Nevertheless, a feedforward topology brings the designers two new challenges: designing low-loss, highly-linear delay circuits and summing circuits. The delay block after the PA may

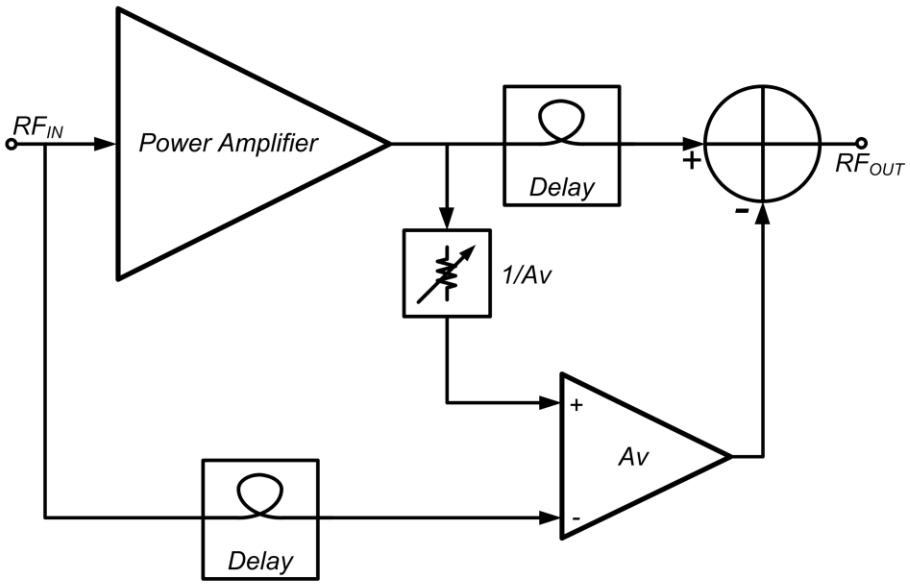


Figure 1.5 The block diagram of a feedforward PA system

have to handle a signal with power up to 30-dBm, which makes passive delay line the only solution. The insertion loss of this passive delay circuit, however, has to be extremely small. At the power level around 30-dBm, 1-dB loss means a waste of power around hundreds of milli-watts, which might be a number larger than the total power consumed by the receiver chain. The other requirement that makes design of a delay line difficult is the area. Passive delay circuits usually include inductors or transmission line structures. These components tend to be bulky at mobile communication frequency, and will dramatically increase the size and cost of the overall PA system. What make things even worse is that the same design issues also apply to the summing circuit.

Even if there are perfect solutions for the delay and summing circuits, the open loop nature makes the PA vulnerable to process variation and electrical performance degradations over time. With the process/temperature variation of the CMOS technology and the degradation comes

from a very large voltage swing cross the devices of a PA, the feedforward topology must incorporate extra blocks to adaptively linearize the PA [4]. However, almost all the proposed adaptive feedforward topology suffers from mismatch between a very complicated adaptive control and feedforward circuits [5]-[8], making the feedforward PA a less practical solution.

1.3.3 Envelope Elimination and Restoration

In an envelope elimination and restoration (EER) PA, the input signal is first fed to an envelope detector as well as to the input of PA, as illustrated in Figure 1.6. Amplitude of the

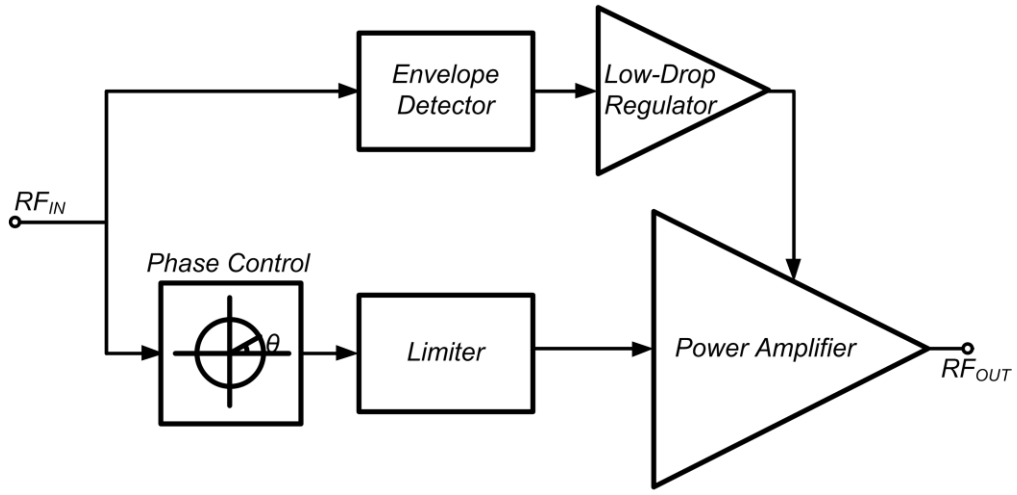


Figure 1.6 The block diagram of a envelop elimination and restoration PA system [3]

signals passing through the latter path will be adjusted to a constant value, remaining only the phase information. On the other hand, the envelope detector will extract the amplitude signal from the very first input, and changing the bias to the PA accordingly so that the envelope at the output of the PA will be proportional to that of the input. A phase shifter is sometimes required in the amplitude limiting path to lower the phase mismatch between two paths and to correct the severe AM-PM conversion from a nonlinear limiter circuit. By separating the amplitude and

phase path, this topology is able to minimize the AM and PM error.

However, this topology suffers from the “zero-crossing” problem. For example, if the PA is designed for WCDMA applications, there will be chances that the envelope of the input signal goes to zero. Therefore, the output of the regulator is required to supply ground bias to the PA. This is almost impossible to achieve with present regulator topology, therefore limiting the EER topology to be only suitable for applications with finite peak-to-minimum power ratio.

1.3.4 Adaptive Predistortion

The idea behind the predistortion is simple: measuring the AM-AM and AM-PM distortion of the PA, and then intentionally adding another distortion that is opposite to the amount of the measured distortion. Because the distortion of a PA varies with process, temperature and output matching, an adaptive predistortion will be much promising for a proper compensation. As illustrated in Figure 1.7, in adaptive predistortion system, a compare and control circuit will measure the amplitude and phase difference at the input and output of a PA. For an ideal linear-

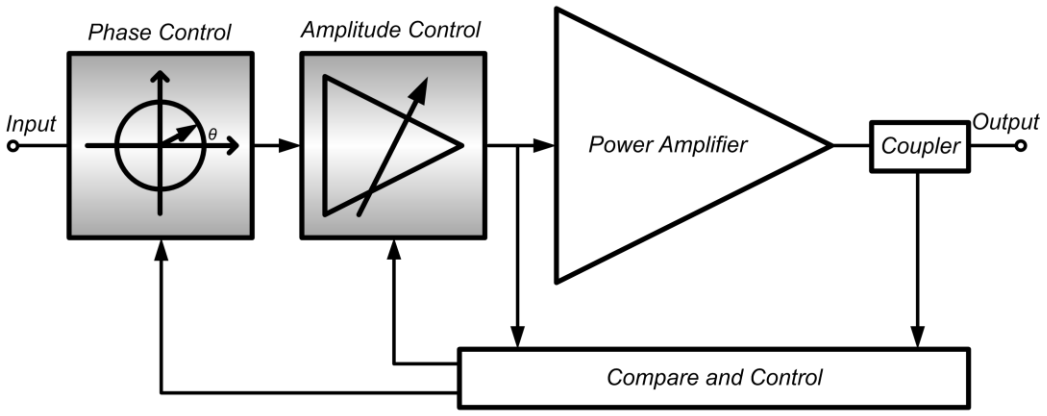


Figure 1.7 The block diagram of a envelop elimination and restoration PA system [3]

PA, the measured differences remain constant regardless off the input; while for a non-linear PA, the differences tend to vary at a higher input power. The compare and control circuit will distinguish the distortion and generate corresponding control signals. These control signals are fed to the phase and amplitude predistorter attached in the input of the PA, changing the phase and amplitude oppositely to the measured distortion. Since the compensation is done at the input, the topology has higher tolerance for the loss as compared to a feedforward topology. Besides, with carefully designed control and compare circuits, oscillation is less probable to occur in the topology.

The control and compare circuit as well as the predistorters can either be implemented in analog or digital domain. Besides, the predistorter could operate either in RF or baseband frequencies. Digital compare and control circuits with baseband predistorters are easier to design and are more reliable over the process and temperature corners. However, this kind of predistortion PA requires high speed, accurate analog-to-digital (A/D) converters, as well as a very linear up-converter to linearly up-convert the predistorted signals to the carrier frequency.

To relieve linearity requirement for the up-converters and remove the power-hungry high speed A/D converters, it is better to operate the predistorters to the RF domain and the control/compare circuits to the analog domain. Furthermore, to reduce the settling time, performing the predistortion through a one-time mapping between the measured error and the amount of gain/phase tuning is much preferable. Such a topology requires a linear-in-dB power detector, a linear-in-dB controlled variable-gain circuit, a linear-in-degree phase detector, and a linear-in-degree controlled variable-phase shifter. Within them, a linear-in-dB controlled amplitude tuning circuit and a linear-in-degree controlled variable-phase shifter are the most challenging parts to design. The difficulties come not just because their input and output signals

are all in at RF frequencies, but also a higher linearity requirement and a small circuit area restriction for them as compared to what they are in their traditional roles.

1.4 Design Challenges for Amplitude Predistortion Circuits

Signal strength control circuits are much commonly find in wireless receiver designs. Transmitting from a remote station and passing through the open space, a signal received by a mobile receiver has relative small amplitude and varies in a wide dynamic range. The function of the amplitude control circuits in the receiver is to map the signal strength to a smaller range that the A/D converters can handle. A large received signal will always be attenuated, while a small received signal is always amplified. The linearity requirement of the amplitude control circuit for such operation is therefore non-uniform. A higher linearity is required at its minimum gain, while a more relaxed linearity is acceptable for the maximum gain. Besides, the signal strength control is usually performed in baseband, which makes them less sensitive to parasitic effects, allowing the control circuits to have more complicated topology with more transistor counts.

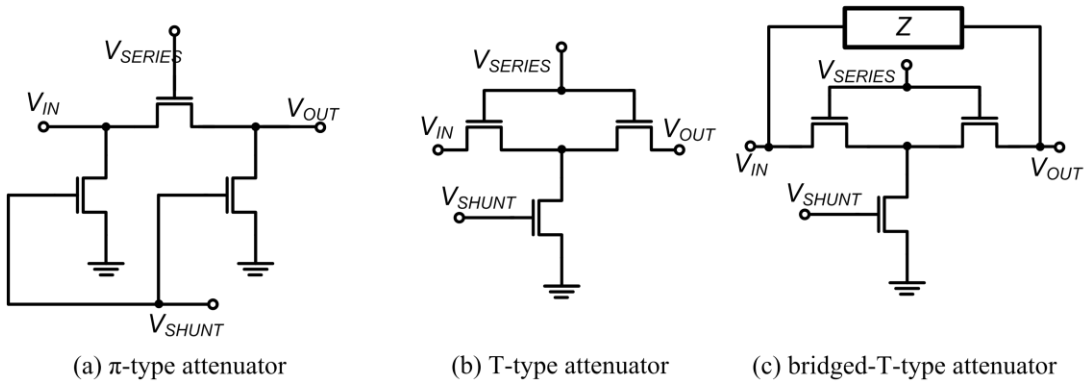
However, an amplitude control circuit in a predistortion system is different. The fore stages of the PA are up-converters and baseband circuits, not an unknown open space. Therefore, the signal strength to the PA is well-controlled, but at a higher power level. In addition, the amplitude control has to be performed at the RF frequency and covers several different bands. The working environment defines the most important characteristics for an amplitude predistorter in an analog predistortion PA: linearity and bandwidth.

There are various types of variable attenuators and VGAs designed to control the amplitude of receiving signals. Their performance may not meet the requirements of the predistortion circuits in a transmitter, but their topologies may give the designer a direction to reach a much

appropriate design. Therefore, the circuit architecture of previous gain control circuits will be introduced, and the deficiency will be explained in this section.

1.4.1 Passive Amplitude Control Circuits

A CMOS attenuator usually uses transistors in their triode region as variable resistors, controlling the ratio of output to input power. Based on the arrangement of series and shunt branches, conventional attenuator topologies can be categorized into π- [9], [10], T- [11], [12], and bridged T- [13]-[14] networks, as illustrated in Figure 1.8. Conforming to similar rules, these



(a) π-type attenuator (b) T-type attenuator (c) bridged-T-type attenuator

Figure 1.8 π-, T-, and bridged T- variable attenuators

topologies entail tunable components connected in series from input to output and consisting of a signal path, thus controlling the flow of passing signals; and tunable components connecting the signal path to the ground, thus diverting the signal.

Figure 1.9 shows a multi-stage π-type attenuator with three series N-type metal oxide semiconductors (NMOS) transistor on the signal path and four shunt NMOS transistors connected from the signal path to the ground. Typically, if the shunt NMOS transistors are controlled by an external signal, the series transistors will be controlled by a feedback circuit that

ensures proper impedance matching [9], [10], and vice versa. For example, the shunt transistors in Figure 1.9 are externally controlled, attenuations can be increased by raising the V_{SHUNT} to reduce the channel resistance of the shunt transistors, thus reducing the isolation from the signal path to the ground. At the same time, a feedback circuit will lower the V_{SERIES} to properly increase the channel resistance of the series transistor until 50-Ω input impedance is reached. The value of the attenuation is determined by the impedance of the transistors, which is composed of

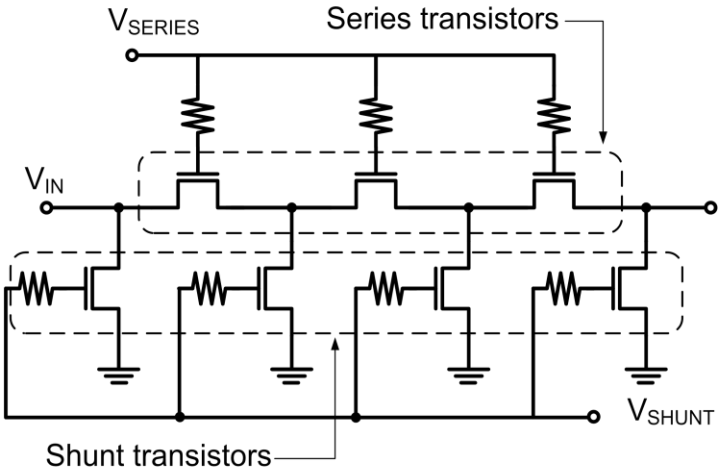


Figure 1.9 A conventional multi-stage π-type attenuator

channel resistance and parasitic capacitance, and is controlled by the bias voltage across certain terminals of the transistors. Therefore, any voltage variation on the terminals of the transistors will change the attenuation value and cause nonlinear gain responses.

As shown in Figure 1.10, one study [11] proposed a method that utilizes multiple control and matching circuits to spread the occurrences of nonlinearity over a wide attenuation range, thereby averaging the power handling capability and improving the minimum IP_{1dB} of an attenuator. The transistor in the proposed attenuator can be grouped into five sets according to the control voltage. Each of the three shunt transistors (M_{SH1}, M_{SH2} and M_{SH3}) have individual

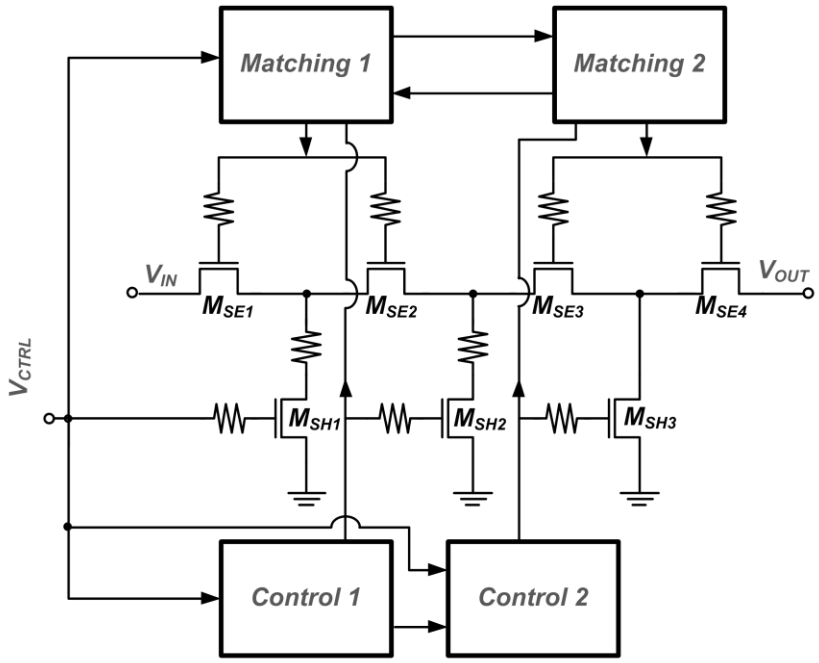


Figure 1.10 A recently reported attenuator design that uses multiple control and matching circuits to spread out nonlinearity of each series transistor [13]

gate control signal, while the first two (M_{SE1} and M_{SE2}) and the last two (M_{SE3} and M_{SE4}) series transistors are controlled by different feedback loops. This configuration allows the transistor in each of the group to be biased in different regions. Therefore, for any given control signal, there will be at most two transistors operating in the most nonlinear region. While for the attenuator in Figure 1.9, there will be chances that all the series transistor or shunt transistors are biased in their most non-linear region. By reducing the number of transistor simultaneously operating in their most-nonlinear region, this method successfully improves the minimum linearity.

However, due to its complicated control blocks, which include six operational amplifiers (OP-AMPs) and several feedback loops, it may be unsuitable for high-speed operations, increasing the complexity and size of the circuits.

1.4.2 Active Amplitude Control Circuits

Although attenuators are suitable for the cases of controlling very-high-power input signals, the passive nature gives them no gain but only loss. For applications that deals with a smaller power in the input of PAs, for example, 0 dBm for most of the WCDMA PAs; using VGAs will become possible, and their gain will give some flexibility to the overall predistortion system design. Various VGA topologies have been reported for receivers and for baseband operation. In contrast with an attenuator, a VGA can provide both gain and attenuation and have much broad application in communication systems. Based on the design considerations of the amplitude predistortion circuits in a transmitter, the characteristics of different baseband VGA topologies will be analyzed in this section.

All VGAs are first characterized in to two kinds according to their control mechanisms. Digitally controlled VGAs utilize binary-select arrays of resistors, capacitors or current sources to change the gain in discrete steps; while analog-control VGAs uses variable resistance or conductance circuits to continuously tune the gain. To correct or predistort a modulated signal in the transmitter, a VGA should be able to finely control the amplitude of an input signal within a relatively confined gain tuning range as comparing to a VGA in the receiver. This restricts the use of digital-controlled VGAs because they usually require an accurate A/D converter to reduce the difference between each gain steps. Digital VGAs also generate phase discontinuity when switching from different gain setups. This is expected to cause problems if the transmitted signals are phase-modulated [15]**.** Therefore an analog-controlled VGA is much preferable for the proposed application.

Linear-in-decibel gain control curve is the other feature desired by VGAs in a gain-control loop. It allows the VGA to have a larger dynamic range and the detection-and-compensation to

be done in a one-time mapping, reducing the settling time. There are various VGA topologies that demonstrate linear-in-dB controlling ability. Their linearity, bandwidth, and noise figure are significantly influenced by the gain control mechanism. Therefore, not all of them are suitable for wideband, large signal and low noise operation.

Figure 1.11 (a) is a source degeneration type VGA. It seems easy to implement but requires extra circuits to generate an exponential control signal to change the channel resistance of the degeneration transistor (M_{DEG}) appropriately. Besides, the size of M_{DEG} should be very large so that its "ON" resistance does not reduce the maximum gain too much. The topology also suffers from limited voltage headroom and poor linearity [16]. Figure 1.11 (b) is a popular linear-in-dB topology for its simple control block. The differential gain of circuit (b) depends on the ratio between the transconductance (g_m) of $M_{N,\,GAIN}$ to that of $M_{N,\,LOAD}$. This ratio is controlled by two complementary current sources and approximately in proportion to an exponential function [17]-[19]. However, the square root approximation of the control circuit limits this VGA's linear-in-dB gain control range to be around 12 dB [16] per stage. Its diode connected load ($M_{N,\,LOAD}$) also adds comparably large parasitic capacitance that reduces the bandwidth. These loads also require larger voltage headroom to be biased in the saturation region, thereby limiting the output voltage swing and linearity. All the disadvantages make it inappropriate to be used in RF predistortion applications.

The *R*-*r* VGA shown in Figure 1.11 (c) uses a set of variable resistors (*r*), which are made with transistors operated in linear region, along with one fixed value resistor (*R*) to approximate an exponential function [20], [21]. Its voltage gain (*Av*) can be expressed as

$$A_V = g_m \times \frac{1}{\frac{1}{R}+\frac{1}{r}} = \frac{g_m \times R}{1+\frac{R}{r}} \approx g_m \times \exp\left(\frac{-2R}{r}\right) \qquad (1.5),$$

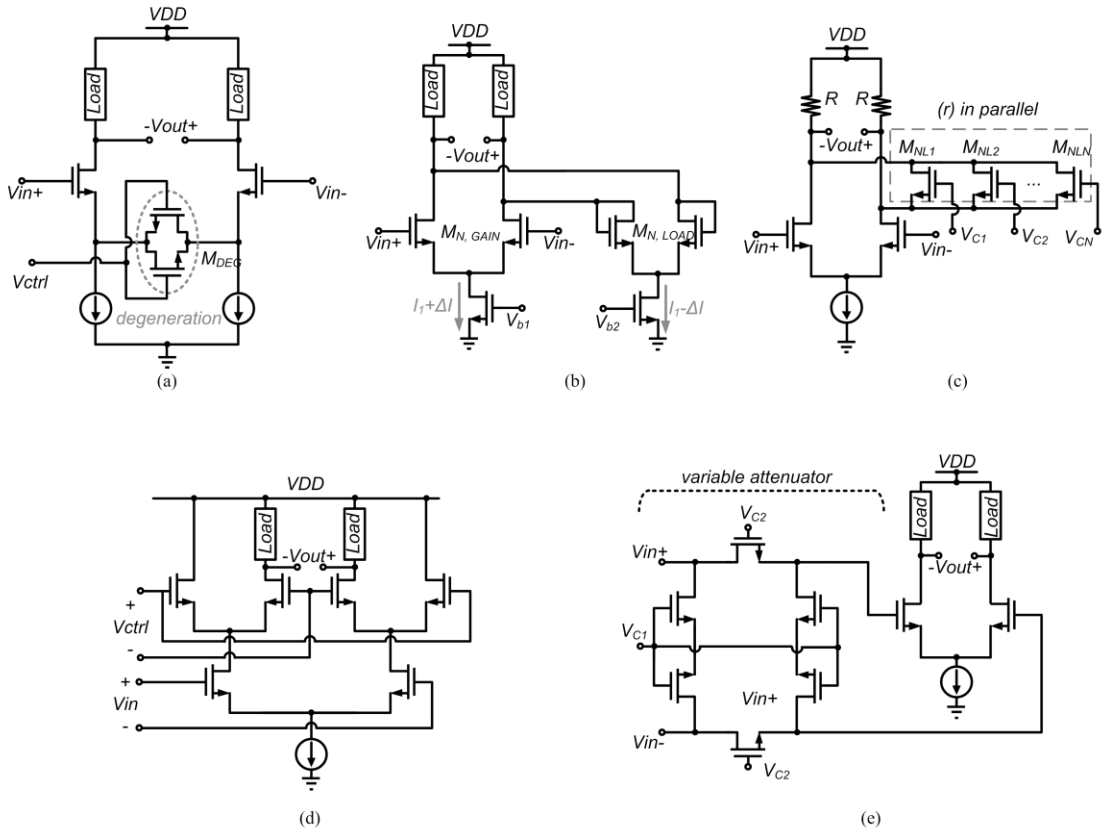


Figure 1.11 Several reported linear-in-dB VGAs

where g_m is the transconductance of $M_{N,\ GAIN,}$ and r the overall resistance of the variable resistors M_{NL1} to M_{NLn}. Since transistors M_{NL1} to M_{NLn} are biased in triode region, $1/r$ is linearly related to their gate bias. Thus, the gain of the *R-r* VGA has linear-in-dB relationship with the gate control voltage of M_{NL1} to M_{NLn}. Its linear-in-dB control error and gain range are determined by the number of unequal sizing variable resistors (r). More "*r*-transistors" gives much accurate and broad linear-in-dB control range but produces higher parasitic capacitance, making it difficult to have enough bandwidth and gain range at the same time.

Adjusting bias current with an exponential control circuit is another popular control mechanism for linear-in-dB VGA [21], [22]. Such VGA designed with metal-oxide-

semiconductor field-effect transistors (MOSFETs) is shown in Figure 1.11 (d). Since MOSFETs are square law devices, common-gate (CG) stages that added to steer the bias current should either be controlled by an exponential function generator or biased in the sub-threshold region. The former method consumes extra DC power, while both solutions need larger voltage headroom for CG stage. Linearity degradation of this kind of VGA is therefore becoming its main disadvantage [16].

Attenuator based VGAs are an option for applications require good linearity. Figure 1.11 (e) illustrates a typical implementation of such VGA. Variable attenuators are put in the input to change the signal strength, and a second variable or fixed gain stage is used to provide sufficient gain [10], [23]. Since the input attenuator carries large burden of gain tuning and reduces the input power, the amplifier stage can have smaller gain tuning range and handle lower input power. Smaller gain tuning range for an amplifier means less DC bias variation, while lower input power relaxes the voltage swing requirement. Both help increase the overall linearity of the VGA. The main tradeoff for its good linearity is a poor noise figure results from resistive attenuator. Although noise performance may seem not critical for transmitters, poor noise figure of an attenuator based VGA is still undesired as long as there is a noise level specification to meet. Except for noise figure, the attenuator based VGA has most of the features the predistortion circuit requires, making it an excellent candidate for controlling the amplitude in a linear PA system.

1.5 DESIGN CHALLENGES FOR PHASE PREDISTORTION CIRCUITS

In addition to amplitude control circuit, a phase control circuit in a prediction PA is of equal importance. A variable phase shifter is the circuit that could perform the function. Phase control

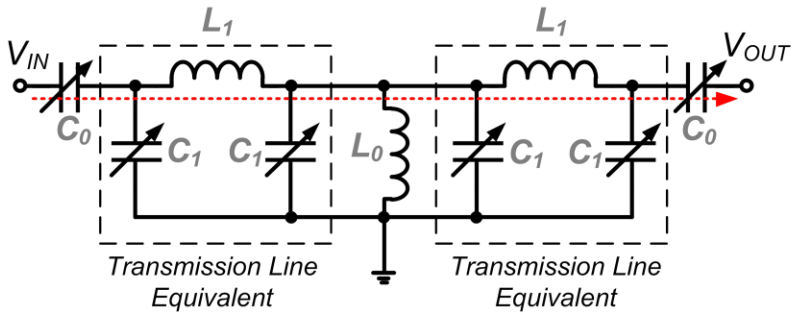
circuits are, unlike original amplitude control circuit, originally used in millimeter-wave phase-array/beam-forming system. They are usually put before the PA to adjust the direction-gain of a transmitted signal. The frequency can be of an order higher than the mobile applications. However, since they are put in front of a PA already in such application, their linearity performance is not an issue if used as a predistorter. The problem is size and power consumption.

For a passive phase shifter, it usually uses several inductors and capacitors to manipulate the phase signal. Inductors are bulky structures, and a VPS made with several inductors is expected to be sizable. Using active equivalents could avoid using such bulky components, but raise the power consumption issue. Several traditional passive and active phase shifters will be introduced later in this section. By investigating their structure, it is possible to find the best tradeoff between power and size, and thereby giving a direction to how to design a phase shifter that fits the requirement of a phase predistorter.

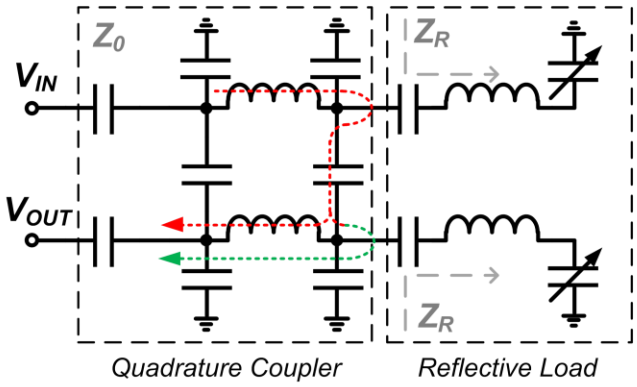
1.5.1 Passive Phase Control Circuits

All the previous passive phase control circuits utilize certain structures to manipulate the phase. These structures might be any kind of coupler or sections of transmission line. Generally, their sizes are inversely proportional to the operation frequency. Therefore, a very bulky circuit is expected if we directly adapt the same phase-shifting topology using in millimeter-wave application to the mobile communication frequencies. To shrink the size of such passive structures to a range that is possible for on-chip implementation, a common way is to use inductors and capacitors to approximate the electrical behavior of a coupler or a transmission line. Two types of phase shifter structure frequently found in the recent literature are synthetic transmission line phase shifter and reflection-type phase shifter (RTPS).

A general topology for both types of phase shifters is shown in Figure. 1.12. They can be easily differentiated by the role of the LC components in them. In a synthetic transmission line



(a)



(b)

Figure 1.12 (a) A phase shifter designed with synthetic transmission lines, and (b) a passive reflection-type phase shifter (RTPS)

phase shifter, as plotted in Figure 1.12(a), LC components are put together and tuned to simulate the electrical behavior of transmission lines with different electrical length. The phase shifts, φ, of circuit in Figure 1.12(a) can be calculated as [60]:

$$\varphi \approx \frac{\sqrt{2}}{\omega\sqrt{L_1 C_1}}\left[1-\omega^2 L_1\left(C_0+C_1\right)\right] \qquad (1.6).$$

Since it is hard to design tunable inductors on-chip, varactors are often used in such phase shifter. By changing the capacitance value of varactors in Figure 1.12(a), we could change the phase of the input signals.

On the other hand, LC components are utilized to build a coupler and reflective loads in a RTPS, as illustrated in Figure 1.12(b). Those LC-loads reflect the input signal with different amplitude and phase. Two reflected signals from different loads will be added up at the output of the coupler. By changing the capacitance value, the phase of the reflected signal at both loads changes, and so does the phase of the output. The phase of such a circuit can be calculated as [24]:

$$\varphi = -180 - 2\tan^{-1}\left(\frac{Z_R}{Z_o}\right) \quad (1.7),$$

where Z_R is the impedance of the reflective load and Z_0 the characteristic impedance of the quadrature coupler. Again, varactors are often used in the reflective load design than tunable inductors.

Since these phase shifters are composed mainly of passive components, they usually have very good linearity. The disadvantage, however, is the size. Because of the bulky inductors, most of the reported synthetic transmission line phase shifters or RTPS operating near the mobile communication frequencies have a size close to that of a PA, as listed in Table 1.2 and Table 1.3. It means if those phase shifters are incorporated in an analog predistortion PA system, the size of the overall system is expected to be at least twice of the size of the PA core. Doubling the size doubles the price, and the CMOS PA system with such passive VPS will lose its “low-cost” advantage over an III-V compound PA, defeating the purpose of using CMOS technology. Therefore, a passive type VPS seems to be not suitable for predistortion applications. It is necessary to find an alternative way to implement the phase predistorter.

Table 1.2 Recently reported WCDMA/EDGE PA

References	Freq (GHz)	Pout (dBm)	Gain (dB)	Size (mm_2)	Application
Wang, JSSC 07[62]	1.75	24	23.9	1.4	WCDMA
Pinon, ISSCS 08[63]	1.95	27	25	1.1	WCDMA
Choi, TMTT 09[64]	1.88	29	27.8	3.5	WCDMA
Jeon, RFIC 10[65]	1.95	26	26	0.832	WCDMA
Choi, TMTT 09[64]	1.88	27.8	29.4	3.5	EDGE

Table 1.3 Recently reported CMOS phase shifter operating at lower GHz

References	Freq (GHz)	Phase Range	Power (mW)	Area (mm^2)
Zarei, ISSCC 04[59]	2.27 - 2.45	105	1.8	1.08
Zarei, ISSCC 04[59]	2.27 - 2.45	105	0	1.08
Zarei, TCAS 07[24]	1.85 - 2.05	360	0	2.5
Zarei, TCAS 0 [24]	1.85 - 2.05	360	2.16	2.5
Wu, TMTT 08 [58]	2.44 – 2.55	340	0	0.66
Wu, TMTT 08[58]	2.33 – 2.60	120	0	0.72

1.5.2 Active Phase Control Circuits

Since bulky inductors are the origin of the size problem, it is reasonable that the first attempt of reducing the size of a VPS is to minimize the inductors. The size of a passive inductor is basically limited by the physical attribute of CMOS process and cannot be reduced easily by design techniques. Therefore, using an active inductor might be a more probable method. One of the common implementation of an active inductor is a gyrator. Connecting two g_m stages in a loop, the circuit in Figure 1.13 is able to approximate the electrical property of an inductor with some parasitics. The inductance value L can be written as [60]:

$$L \approx \frac{1}{g_{m1}g_{m2}}\left[C_{in2}\left(1+\frac{R_F}{R_1}\right)+C_1\right] \quad (1.8),$$

and the series resistor R_S that determines the quality factor of the active inductor can be written as [60]:

$$R_S \approx \frac{1}{g_{m1}g_{m2}}\left(\frac{1}{R_1} - \omega^2 C_{in2} C_1 R_F\right) \tag{1.9}$$

Such an active inductor can be used to replace the shunt inductors in a passive VPS. Its quality factor can be higher than 50 at certain frequencies, and with carefully designed g_m stage. For the same VPS structure in Figure 1.12, we could replace the inductor, *L*, in (a) or the inductor of the

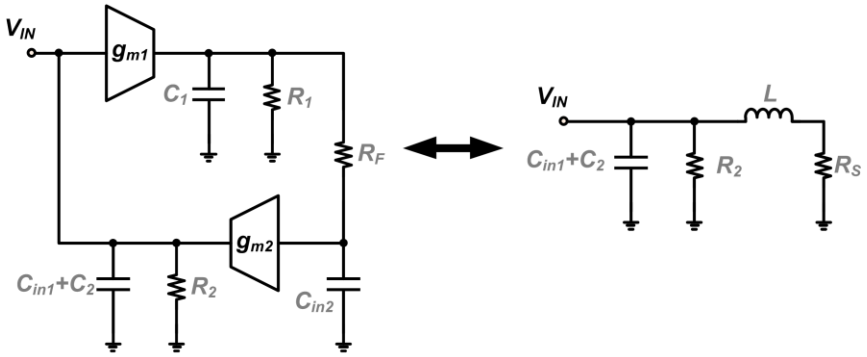


Figure 1.13 Implementation of an active inductor

reflective loads in (b) (but for RTPS, one should exchange the inductor location with varactor so that it could be connected to ground) to reduce the overall size of the VPS. However, series inductors in the VPS still have no active substitutes, limiting the effectiveness of size reduction by active inductors.

Figure 1.14 demonstrates another solution for minimizing the size of a VPS [25]. In addition to using active inductors in the reflective loads, this design replaces the passive coupler in a traditional RTPS with an active circulator. The specially designed active circulator alone with the active inductors successfully reduces its size to be one-third of a traditional passive-RTPS. However, to maintain a reasonable linearity, this all-active VPS consumes a power more than 100-mW. If it is used as a phase predistorter, the efficiency of the overall predistortion PA system will be degraded dramatically.

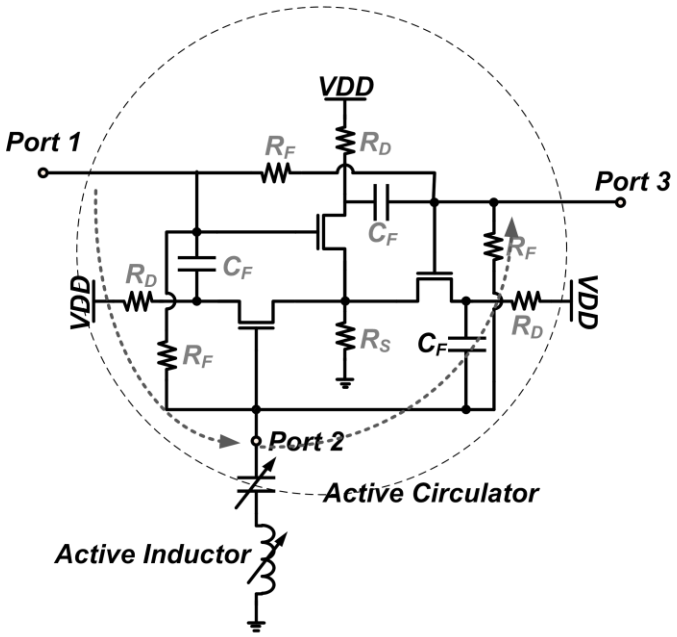


Figure 1.14 The schematic diagram of an all active phase shifter

The third way of implementing an active VPS is called forward-type phase-shifter (FTPS), or sometimes, a vector-sum type phase shifter. As shown in Figure 1.15, such a VPS utilizes

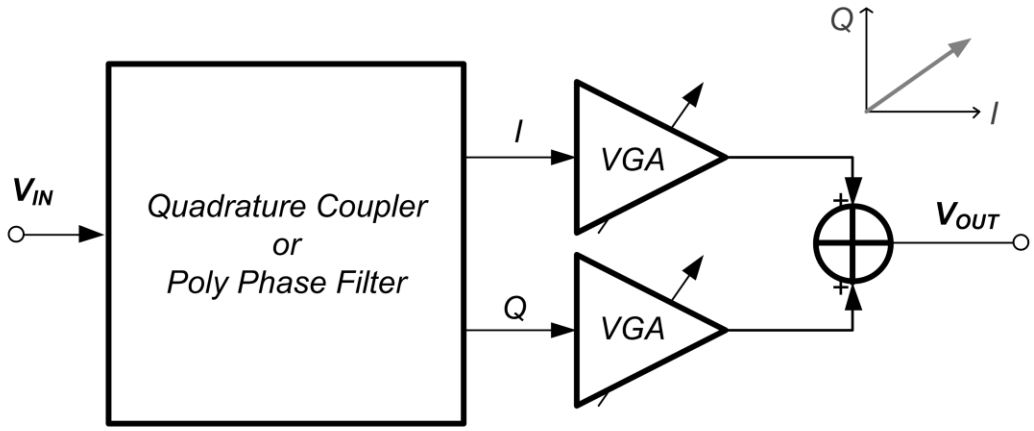


Figure 1.15 The schematic diagram of a vector-sum type phase shifter (or FTPS)

passive circuits (usually a quadrature coupler for single-end input, or a poly-phase filter for differential input) to generate an in-phase (I) and a quadrature (Q) phase vector. The amplitude of these I and Q vectors will be controlled by two VGAs and then combined by a summing circuit. By changing the magnitude of I and Q vector, the phase of the output will be changed. The advantage of a FTPS is that a quadrature coupler can be easily implemented with 2 or less inductors and needs no tunable reflective loads. In addition, the VGA circuits consume less power than the active inductor and the active circulators, while having better stability. Besides, the output magnitudes over the phase shifting range are much well-controlled than any RTPS, contributing less amplitude errors to the overall predistortion system. All these features make the FTPS a more attractive topology for the analog predistortion PA system.

1.6 DISSERTATION OUTLINE AND ORIGINAL CONTRIBUTIONS

The remainder of this dissertation is organized into five chapters. The first three chapters mainly focus on developing and analyzing the circuit topology for a passive gain control circuit, an active gain control circuit, and an active phase control circuits. General design examples and circuits implemented in a commercial-available CMOS technology will be given in each chapter. The forth chapter demonstrates the simulation results of a predistortion system that adapts the proposed gain- and phase- control circuits in a complete analog predistortion PA system. The last chapter summarizes the work of this research and discusses the possible direction of future works. A more detailed outline of each chapter is given as below:

Chapter 2: A Highly Linear Variable Attenuator for Signal Strength Controlling:

In this chapter, several approaches to design a linear attenuator have been analyzed in terms of the transistor impedance variation, linearity, frequency responses, and circuit complexity. A novel method of using an adaptive bootstrapped body biasing is then presented. The method allows the attenuator to have maximum power handling capability and bandwidth without adding complexity to the circuit. A π-type variable attenuator for WCDMA transmitters has been designed and fabricated using IBM 0.18-*μm* triple-well CMOS technology. Based on the experiment results, this design achieves the best linearity performance and frequency responses, and has the smallest area among similar CMOS works.

Some of this work was published in the *IEEE Radio Frequency Integrated Circuit Symposium*, 2010; and in the *IEEE Journal of Solid State Circuits* vol.46, issue 5, May 2011.

Chapter 3: A Highly Linear Variable Gain Amplifier for Analog Predistortion Systems:

This chapter demonstrates a VGA topology that achieves an optimized linearity and bandwidth performance while having a continuous, linear-in-dB gain control curve. The presented VGA topology employs a self-biased differential amplifier with a dynamic current boosting to provide gain and linearity. The overall VGA gain is then controlled by a highly linear variable attenuator connected at the output of its amplifier. This separated controlling stage allows the VGA to have a continuous and linear-in-dB gain curve without sacrificing the bandwidth and linearity of its amplifier stage. A VGA designed with such topology has been fabricated in a standard 0.18-*μm* CMOS technology. The experiment results of this VGA demonstrate the best linearity performance and have other characteristics that on par with other CMOS VGAs.

Some of this work was summarized and submitted to the *IEEE Transaction on Microwave Theory and Techniques.*

Chapter 4: An Ultra Compact Variable Phase Shifter for Analog Predistortion Systems:

This chapter presents and analyzes a vector-sum type phase shifter topology. The proposed topology is able to have a continuous, linear-in-degree control curve over 90° phase control range and the smallest size among CMOS works. The VPS utilizes a modified RC poly-phase filter to generate the in-phase and quadrature vectors over a wider bandwidth, and has less RC components as compared to traditional RC filters, reducing the loss and size of the overall VPS. A specially designed control circuit gives the VPS a linear phase control curve and minimizes the gain variation over the phase control range. Based on the experiment results, the VPS has a maximum 90° phase control range, and 1 dB gain variation over a bandwidth that covers most of the mobile communication standards. Its linear-control phase errors are less than ±1° in 70° phase control range, making it suitable for accurate AM-PM error compensations.

Some of this work was summarized and submitted to the *IEEE Transaction on Microwave Theory and Techniques.*

Chapter 5: A Multiband Analog Predistortion Power Amplifier in CMOS Technology

A system level simulation is demonstrated in this chapter to verify the effectiveness of the proposed amplitude and phase control circuits in an analog predistortion PA system. Most of the blocks in the system are designed in the same CMOS technology. This includes a variable phase shifter, a variable gain amplifier, a 2-stage power amplifier, a power detector, and a part of a phase detection loop. The remaining blocks are behavior models built according to the real characteristics of corresponding circuits. The simulation compares the AM-AM, AM-PM error and other linearity performance between a non-linear PA with and without predistortion circuits.

Chapter 6: Conclusions

This chapter gives the summary of the research, and the suggestions for future work.

CHAPTER 2

A HIGHLY LINEAR VARIABLE ATTENUATOR FOR SIGNAL STRENGTH CONTROLLING

2.1 INTRODUCTION

As mentioned in previous chapter, variable attenuators are inherently much linear than VGAs due to their passive nature, making them excellent candidates for manipulating large signals. There is the other reason that attenuators are suitable for the role- their small power consumption. While CMOS VGA usually fails to meet the required linearity unless it consumes tens or even hundreds of milliwatts of power [11], most of the reported attenuator designs have an IP_{1dB} of as much as several dBm [11], [26] with DC power consumptions as low as 2 mW [11]. Therefore, the research starts first with the attenuator design. The goal is to resolve the control-circuit complexity issue while keeping, or if possible, improving the linearity.

The nonlinear responses of a CMOS variable attenuator such as intermodulation distortions are mainly due to impedance variation. These effects have been well analyzed in a literature using digital CMOS technology [27]. As mentioned in chapter 1, one study [11] proposed a complicated method that utilizes multiple control and matching circuits to spread the occurrences of nonlinearity over a wide attenuation range, thereby averaging the power handling capability and improving the minimum IP_{1dB} of an attenuator.

With triple-well CMOS process prevailing in RF front-end designs, the power handling capability of an attenuator can be enhanced with less complicated and more energy efficient

means. This chapter demonstrates several approaches based on the utilization of the independent body terminal of triple-well devices. In the following sections, these approaches will be analyzed in terms of IP_{1dB}, intermodulation distortion, bandwidth, and maximum attenuation.

2.2 LINEARITY PERFORMANCE OF ATTENUATORS

As mentioned in chapter 1, the worst-case nonlinearity occurs when there are multiple transistors biased in their most-non-linear region, where the transistor has most significant impedance variation. Therefore, for the attenuator circuit shown in Figure 1.9, the nonlinearity is critical in two regions of the attenuation. One is when all the series transistors are nearest to the threshold voltage, the other is when all the shunt transistors are nearest to the threshold voltage. As shown in Figure 2.1, by plotting the IP_{1dB} values at different attenuation region for circuit in Figure 1.9, we could easily observe such phenomenon. Since the impedance variation is the reason, and the transistor impedance are composed of channel resistance and parasitic

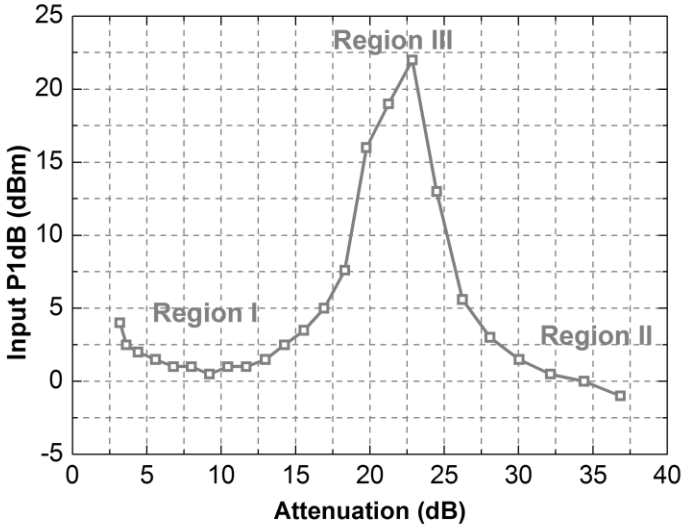


Figure 2.1 IP_{1dB} and critical linearity regions of an attenuator at 1.95 GHz

capacitance, it is reasonable to divide the problem into two parts (channel resistance and parasitic capacitance) and solve them separately.

The variation of the channel resistances in each region can be explained with the channel resistance model [11], [28-29],

$$R_{CHANNEL} = \frac{1 + \theta\left(V_{GS} + \Delta v_{gs} - V_{TH}\right)}{\mu C_{OX}\left(\frac{W}{L}\right)\left[V_{GS} + \Delta v_{gs} - V_{TH} - \eta\left(V_{DS} + \Delta v_{ds}\right)\right]} \quad (2.1),$$

where θ models the drain-to-source resistances and η models the exponential behavior of the drain current in the subthreshold region. In addition, Δv_{gs} and Δv_{ds} represent the AC voltage swing induced by the input signal. Because all the source and drain terminals of the transistors in an attenuator are biased at ground potential (V_S=V_D=0) in the quiescent state, the V_{GS} can simply be the gate control voltage V_{SHUNT} or V_{SERIES}. In region I (lower attenuations), the V_{SHUNT} is close to the threshold voltage (V_{TH}) of the transistor, so the shunt resistances are large enough to prevent most of the signals from reaching the ground. As the power of the input signal increases, the AC-coupled gate voltage swing (Δv_{gs}) of the shunt transistor increases. Since the V_{SHUNT}-V_{TH} is originally small, a small amount of Δv_{gs} will cause significant variations in the shunt channel resistance. Similarly, the V_{SERIES} is close to the V_{TH} in region II (higher attenuations), and the series channel resistances are susceptible to the amplitude of the input signal. In region III (mid-attenuations), the impedance of the series and shunt transistors have the same variations. Since their impedance contributes oppositely to the attenuation, they cancel out each other's influences on gain flatness, and give the attenuator very good linearity here. Therefore, one of the key issues of improving the worst-case linearity performance is how to reduce the resistance variation in region I and II.

An intuitive method of lowering the resistance variation is to reduce the gate-to-source

voltage swing of each transistor. As shown in Figure 2.2(a), multiple transistors are connected in series to replace the original shunt transistor. The signal swing on this multi-stack-transistor shunt branch will be equally carried by each transistor. This decreases the Δv_{gs} and channel resistance variation of each transistor, thereby improving the linearity. The method is widely

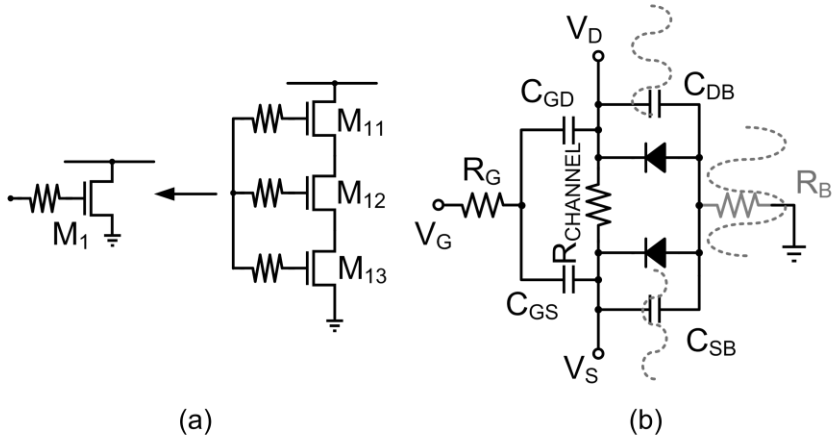


Figure 2.2 (a) A schematic diagram of multi-stack transistors, and (b) the parasitic model of a NMOS transistor with floating body

used in CMOS switch and attenuator designs [30-32], or in the form of multi-gate transistors in several GaAs attenuators [14], [33].

In addition to channel resistance variation, parasitic capacitances are modulated by the input signal and contribute to the degradation of linearity as well. They are also sensitive when the gate bias is close to the threshold voltage. In every attenuator or switch design, it is well known that the influences of the gate capacitance on linearity can be alleviated by large (> 10 kΩ) gate bias resistors. As shown in Figure 2.2(b), the same concept may be applied to the body terminal to suppress the variation of junction capacitances C_{DB} and C_{SB}, which lies on the signal path and directly affects linearity. Since a resistor connecting the body to the bias circuit carries most of the signal swing, the voltage across the drain/source to the body declines. A smaller voltage

swing, which results in a smaller amount of junction capacitance and less variation [30], [31], [34], improves the bandwidth and linearity, respectively.

An attenuator with triple-stack shunt transistors as well as a floating body are simulated and compared to the original attenuator, as shown in Figure 2.3. The results show significant improvement in linearity in region I, but disappointing linearity in region II, indicating that series

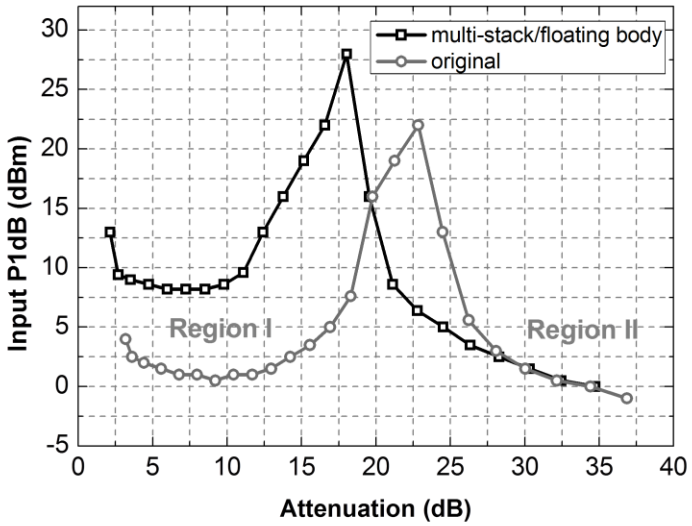


Figure 2.3 IP_{1dB} comparisons between two attenuators at 1.95 GHz

transistors are still susceptible to input power. However, unlike shunt transistors, multi-stack series transistors are largely undesirable because they directly add parasitic capacitance to the signal path in a square relationship. For example, if double-stack transistors are used, the widths of each transistor must be doubled to maintain the same insertion loss in theory. Two transistors with double channel width produce four times as much parasitic capacitance as the original transistor. The added parasitic capacitance not only increases the minimum insertion loss but also significantly reduces the bandwidth in the high attenuation region because series transistors have high resistance here and the cut-off frequency is very sensitive to parasitic capacitance. These

tradeoffs are unacceptable in attenuator design. Therefore, only the floating body technique can be utilized for a series transistor, and the improvement in the IP_{1dB} is insufficient.

Because region II creates a bottleneck in an attenuator design in terms of its power handling capability, a method of both enhancing linearity without sacrificing bandwidth and minimizing insertion loss is required. Otherwise, the minimum IP_{1dB} that is determined by the higher attenuation region will restrict the use of this attenuator at higher input power, and any linearity improvement in the low attenuation region will become meaningless.

2.3 BODY BIASING AND LINEARITY

As previously addressed, nonlinearity arises from two major contributors: variations in parasitic capacitances C_{DB} and C_{SB} due to input signal swings and the coupling effect at the gate, which changes the channel resistance. In this section, resistors are employed to construct a less signal-dependent path to the body terminal of the transistors to further reduce the signal dependency on C_{DB} and C_{SB} as well as to compensate for AC-induced Δv_{gs} through the body effect. Influences on linearization of the reactance and compensation for the channel resistance will be analyzed for different body biasing topologies. In addition, attenuators with different body biasing topologies will be compared later in terms of linearity and maximum attenuation.

2.3.1 Body Biasing and Parasitic Effect

Junction capacitance C_{DB} and C_{SB} can be modeled as [35]

$$C_{DB} = C_{db0} \times \left(1 + \frac{V_{DB}}{\Psi_0} \right)^{-1/2}, \tag{2.2}$$

$$C_{SB} = C_{sb0} \times \left(1 + \frac{V_{SB}}{\Psi_0} \right)^{-1/2}, \tag{2.3}$$

where C_{db0} and C_{sb0} are the zero bias junction capacitance between the source/drain and the body, respectively. Ψ_0 is the built-in potential between the source/drain and the body, and the doping levels are assumed to be constant. In addition to process-dependent parameters, parasitic capacitances vary with the voltage drop across the source/drain and the body, denoted as V_{DB} and V_{SB}, respectively, in (2) and (3). However, AC signals applied to the attenuator change the original bias voltage across the drain/source and body. Since this AC-induced voltage differences are functions of the impedance between drain/source to body and are mainly determined by C_{DB} and C_{SB}, both V_{DB} and V_{SB} in (2) and (3) are no longer constants but functions of the parasitic capacitances. This mutual dependency between V_{SB}/V_{DB} and C_{SB}/C_{DB} leads to inconstant parasitic capacitances and gain variations in an attenuator. In order to suppress such variation, V_{DB} and V_{SB} have to remain constant regardless of the parasitic effect.

Referring to CMOS switch designs, the body terminal of a transistor at receiver side may be connected to the source to change the impedance of the switch, and to prevent channel formation from large signals at the receiving port of the switch when operating under the Tx mode [30]. The concept of intentionally controlling the body voltage may also be applied to an attenuator design. However, the body voltage control concept applied to the attenuator design is for utilizing the input signal to compensate for the impedance variation, not for blocking unwanted signals as in the case of switch design. A simple circuit implementation of this bootstrapped body biasing is a resistive path connected from drain to body, as shown in Figure 2.4. Because resistors in CMOS technology are almost invariant to the voltage drop across them,

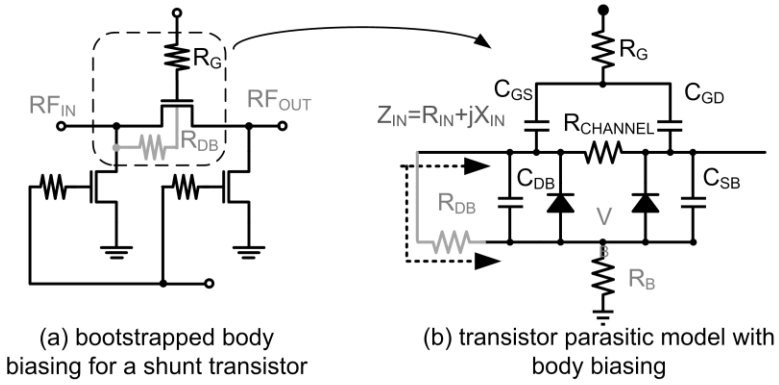


Figure 2.4 Bootstrapped body biasing by a resistor on a shunt transistor

they can help reduce the signal dependence of parasitic effects.

The effectiveness of resistive bootstrapped body biasing was demonstrated in a simulation that compares three 3-stage π-type attenuators with different body biasing topologies. The size of the transistors in each attenuator is the same, and the values of the attenuations are equal. The reactance values are obtained at the same stage of series transistors in each attenuator. The resistance of the R_{DB} used in the body connected attenuator is around 150 Ω, and its impedance is smaller than that of the C_{DB} at a lower gigahertz frequency, so the amount of coupling voltage at the body strongly relies on the R_{DB}. The reactance variation with input signal power is shown in Figure 2.5. The reactance of a transistor with a grounded body terminal exhibits a 57% variation over the power range, while a floating body reduces the variation to 20%, and a resistive bootstrapped body biasing further suppress the variation to 9.5% over the same input power range. This indicates that a resistive bootstrapped body biasing is an effective way of decreasing the reactance variation.

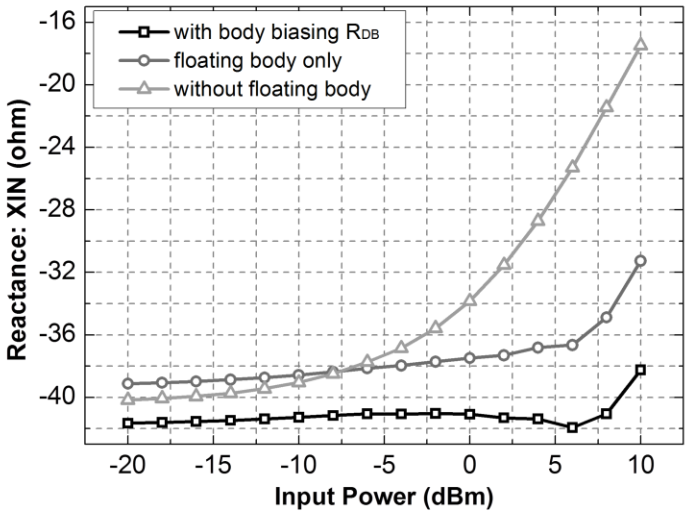


Figure 2.5 Simulated reactance of the same series transistor in attenuators with different body biasing at 30-dB attenuation and at 1.95 GHz

2.3.2 Body Biasing and Channel Resistance Variation

The reactance variation has been successfully suppressed, but the channel resistance variation remains a problem. Fortunately, bootstrapped body biasing in Fig. 5 can also reduce the channel resistance variation resulting from the AC swing of the gate-to-source voltage difference. As shown in (1), the $R_{CHANNEL}$ varies according to the signal strength dependent term Δv_{gs} while the V_{TH} is a constant. However, with the triple-well device, the V_{TH} can vary if the body voltage is manipulated. Variation in the V_{TH} results from the difference in the body-to-source voltage, which can be calculated from [36]

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\left|2\Phi_f + V_{SB}\right|} - \sqrt{\left|2\Phi_f\right|}\right) \qquad (2.4),$$

in which γ is the threshold voltage parameter, Φ_f is the surface potential, V_{TH0} is the threshold voltage for zero body biasing, and V_{SB} is the source-to-body voltage difference.

Being intentionally coupled to the body, the input RF signal will modulate the V_{TH} as it modulates the gate signal, and changes the V_{TH} term in the channel resistance equation (1) to V_{TH} $+\Delta v_{th}$. Fig. 7 shows the calculated channel resistance based on the 0.18-μm RF CMOS

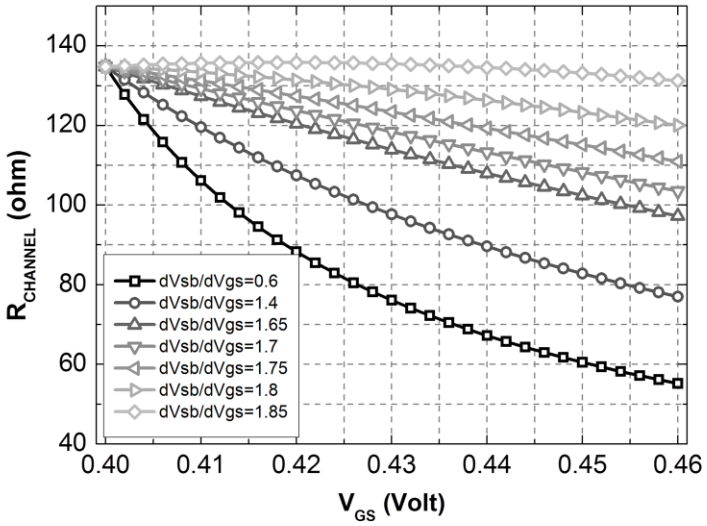


Figure 2.6 Calculated channel resistance over a V_{GS} variation with different dvsb/dvgs values

technology parameters. The V_{GS} values in (1) are set to be close to the V_{TH0} while the drain-to-source voltages are assumed to be constant. Since Δv_{gs} and Δv_{sb} are approximately linear to the input signal, $\Delta v_{gs}/\Delta v_{sb}$ is a constant that is determined by the coupling ability of body biasing. As shown in Figure 2.6, a different $\Delta v_{gs}/\Delta v_{sb}$ ratio reduces $R_{CHANNEL}$ variation differently, and a specific ratio could maintain a relatively constant $R_{CHANNEL}$ over a broad range of Δv_{gs}.

Circuit simulations show the effect of bootstrapped body biasing on reducing the variation in channel resistance. Three attenuators consisting of identical transistors are connected in different topologies: (a) without a floating body, (b) with only a floating body, and (c) with a resistive bootstrapped body biasing. Each attenuator is set to have an attenuation of 30 dB, which is around the power handling limitation of region II in Figure 2.3. The channel resistance values are

obtained at the same series stage of each attenuator. The results, shown in Figure 2.7, indicate that without a floating body, the resistance exhibits about a 45% variation over the simulated input power level. A floated body reduces the resistance variation to 10%, while the resistive bootstrapped body biasing can further reduce resistance variation to less than 2%. As the channel resistance over input power levels being flatten, a relatively linear attenuation response is expected in region II.

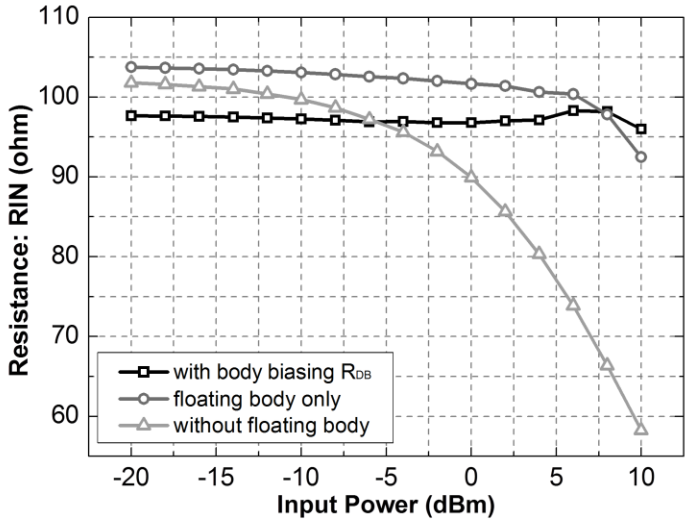


Figure 2.7 Simulated channel resistance of the same series transistor in attenuators with different body biasing at 30-dB attenuation and at 1.95 GHz

However, bootstrapped body biasing with a fixed resistance couples excessive AC signal swing to the body at lower attenuation region I. As demonstrated in Figure 2.8, the channel resistance is obviously over-compensated by an excessive body voltage swing at the 10-dB attenuation. Therefore, the proper linearization of channel resistance at different attenuation regions necessitates a topology that can adaptively change the amplitude of the source-to-body voltage.

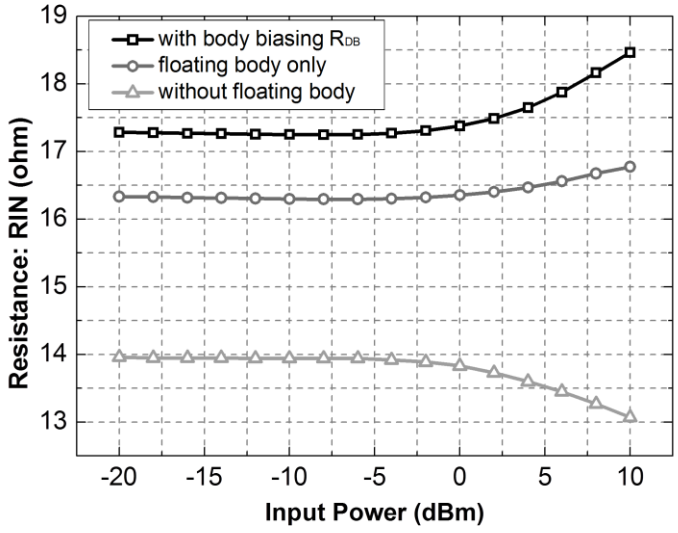


Figure 2.8 Simulated channel resistance of the same series transistor in attenuators with different body biasing at 10-dB attenuation and at 1.95 GHz

2.3.3 Derivative Body Biasing Topologies and Their Linearity

Variable resistance components, as the schematic diagram shows in Figure 2.9(B), may be an intuitive solution for adaptive body biasing. By controlling the body biasing resistance at different attenuation settings, various amount of signal coupling can be achieved. At lower attenuation settings, large body biasing resistances are required to reduce the source-to-body swing (body voltage is closer to the source with a large R_{DB}), and at higher attenuation settings, small body biasing resistance values can help compensate for the channel resistance variation of a MOSFET. Variable body biasing resistors can be implemented with carefully-sized transistors such as MOSFETs or BJTs. If n-type devices are used, the gate/base control signal needs to be low at lower attenuation settings and high at higher attenuation settings to appropriately change the resistance between the drain and the body. Control signals can simply be the V_{SHUNT} because

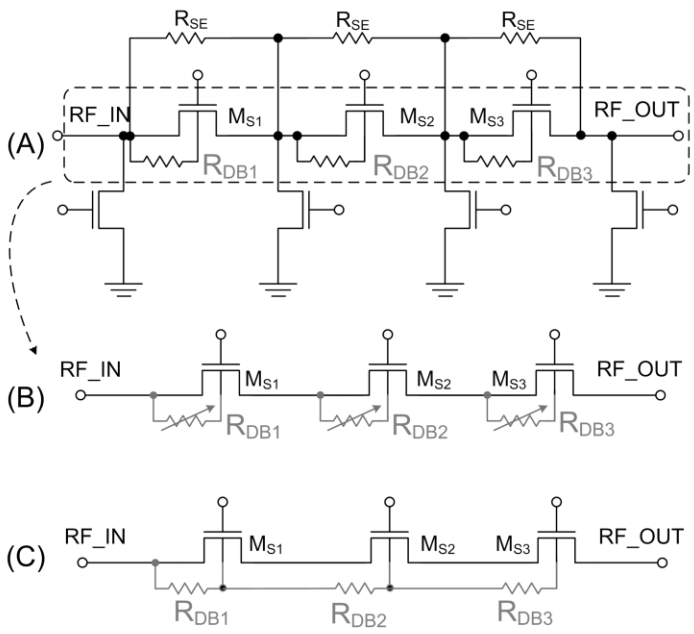


Figure 2.9 Derivative bootstrapped body biasing topologies. (A) Body biased by resistors, (B) adaptively biased with tunable resistive components, and (C) adaptively biased with resistors. Although no R_{SE} is shown in (B) and (C), identical transistors are used in every attenuators design mentioned in this paper.

shunt transistors tend to vary in a similar manner at different attenuation settings. The tradeoffs of this method are that transistors usually require a larger area than resistors and their gate control lines complicate the wiring in physical layout.

A less complicated method of realizing adaptive body biasing in multistage attenuators is presented in Figure 2.9(C). Body biasing resistors M_{S2} and M_{S3} are connected at the body terminal of the forestage instead of at the drain of M_{S2} and M_{S3} themselves. Hence, the body voltage swing of M_{S2} and M_{S3} is determined by both their body biasing resistors and the impedance of the forestage transistor. For example, the impedance of R_{DB1} plus R_{DB2} is much larger than M_{S1} at low attenuation region I, thereby allowing only a small amount of signal

passing through R_{DB1} and R_{DB2} to the body terminal of M_{S2} and inducing only a small body-to-source swing. Conversely, the impedance value of R_{DB1} plus R_{DB2} is much smaller than that of M_{S1} in high attenuation region II; hence, a larger voltage swing is coupled to the body of M_{S2}. Figures 2.10 and 2.11 show that with adaptive bias (C), the channel resistance can be properly compensated for in both attenuation regions I and II. In addition, topology (C) requires no extra control signals and utilizes only fixed value resistors; thus, it is easier to implement than

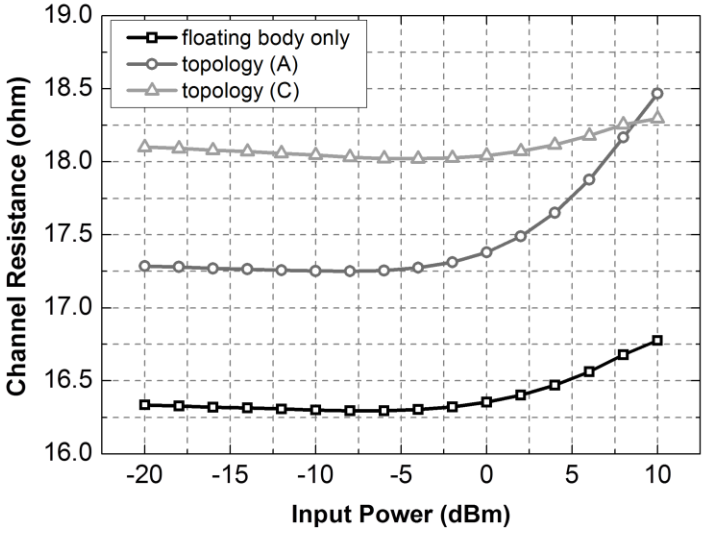


Figure 2.10 Channel resistance variation of different body biasing at 10-dB attenuation and at 1.95 GHz

topology (B).

Another benefit of topology (C) is that the source-to-body voltages of M_{S2} and M_{S3} are not limited by their drain voltage swings, providing topology (C) with enough Δv_{th} to compensate for resistance variation under a larger amount of signal power in region II, but at the risk of compromising linearity performance in region I due to a lack of adaptive body biasing for M_{S1}.

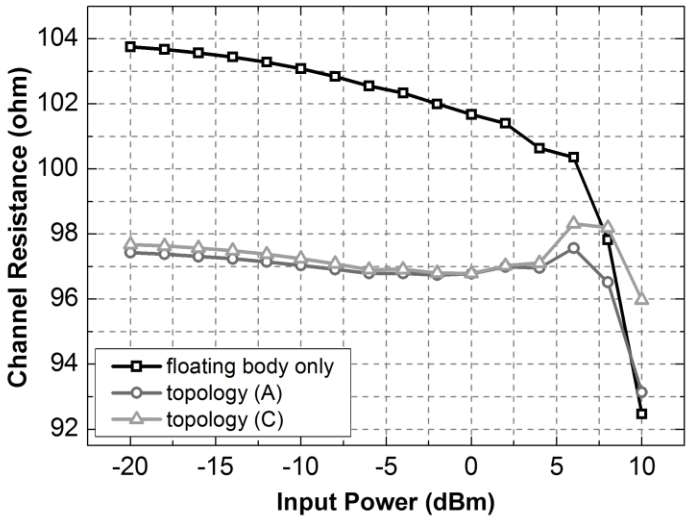


Figure 2.11 Channel resistance variation of different body biasing at 30-dB attenuation and at 1.95 GHz

Figure 2.12 and 2.13 are the simulated results of IP_{1dB} for different attenuator topologies with the same transistor design parameters. Compared to that of the attenuator with only floating body technique, the worst-case IP_{1dB} of topology (A) is increased by 1 dB with a 150-Ω body biasing resistor. With an identical resistance value, topology (C) has a worst-case IP_{1dB} 2 dB better than that of topology (A). Topology (C) also increases the IP_{1dB} in the lower attenuation region by reducing the channel resistance overcompensation of the series transistor. It should be noted that the multi-stack shunt transistors dominate linearity at a low attenuation, and therefore any improvement in the compression point due to bootstrapped body biasing is less than 1 dB.

The final design is optimized based on topology (C), and its linearity is also compared in Figures 2.12 and 2.13. R_{DB1} is shorted (0 Ω), while the value of R_{DB2} and R_{DB3} are selected to further increase the source-to-body voltage swing and the threshold augmentation in high attenuation region II in this design. The linearity degradation in region I is minimal, but the IP_{1dB}

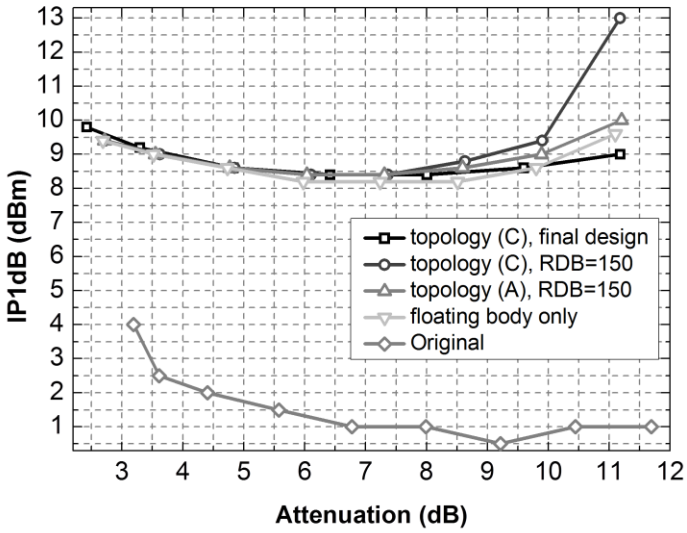


Figure 2.12 IP_{1dB} comparison of different body biasing topologies at lower attenuation settings (region I) and at 1.95 GHz

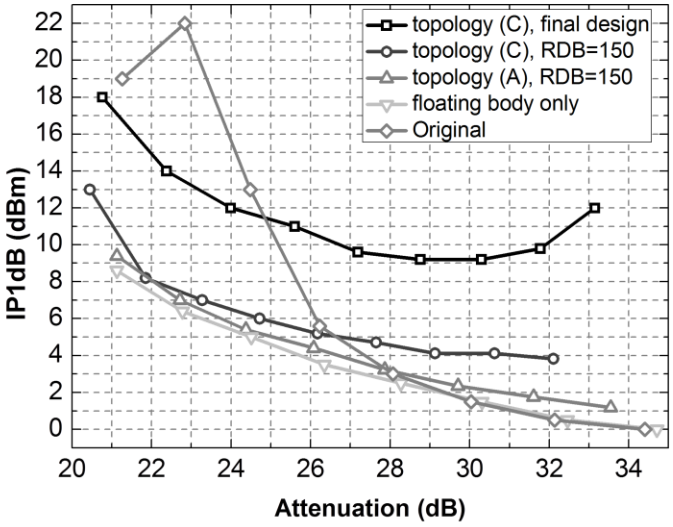


Figure 2.13 IP_{1dB} comparison of different body biasing topologies at higher attenuation settings (region II) and at 1.95 GHz

in region II is about 5 dB higher than that of the original topology (C), increasing the worst-case IP_{1dB} of the final design by at least 8 dB more than that of a 3-stage, π-type variable attenuator

with only floating body.

To examine the intermodulation distortion of the final attenuator design, this study also performs a two-tone simulation. The frequencies of two input signals are 1948.5 MHz and 1951.5 MHz, which are within WCDMA band I (1920-1980 MHz). The tone spacing is selected to be slightly less than the WCDMA bandwidth specification (3.84 MHz). Figure 2.14 compares the output power of 1st- and 3rd-order terms to that of an attenuator using only a floating body and multi-stack transistors. Bootstrapped body biasing not only pushes the compression point of the 1st term to a higher input power, but also lowers the 3rd term by more than 10 dB at 0 dBm input power. As a part of the transmitter, the proposed design hereby relieves the adjacent channel leakage requirement of the following stage, usually a PA.

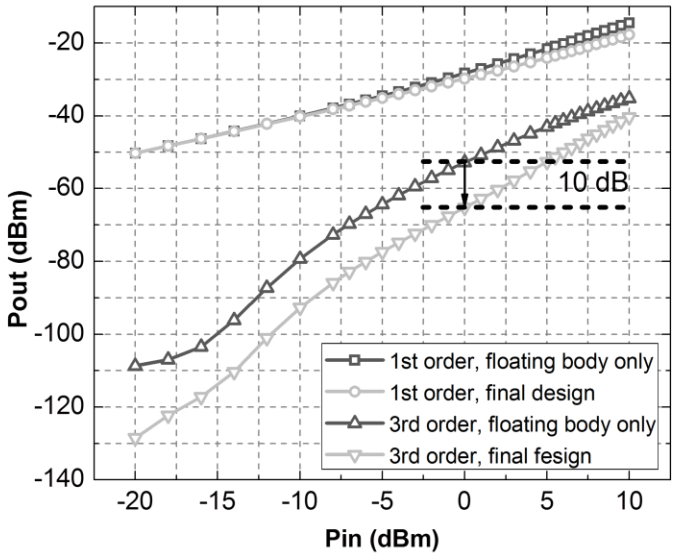


Figure 2.14 Simulated output power and IMD_3 over input power, with 1948.5 MHz and 1951.5 MHz input signals; attenuation is 30-dB for both attenuators

2.3.4 Maximum Attenuation and Frequency Response

The IP_{1dB} improvement of topology (C) has another tradeoff. Figure 2.15 shows the

frequency response of topology (C) with different R_{DB} values. Adding R_{DB} to the attenuator also adds a low-frequency zero and a pole to its frequency response. The location of the zero is mainly determined by the source-to-body capacitance of the last series transistor, regardless of the R_{DB} value; however, the frequency of the pole decreases as the R_{DB} values increases. With an infinitely large R_{DB}, the pole will move infinitely close to the zero, and they cancel out each other; but the proposed bootstrapped body biasing requires a small R_{DB}, which shapes the frequency response of an attenuator into that of a band-pass filter. This small R_{DB} reduces the

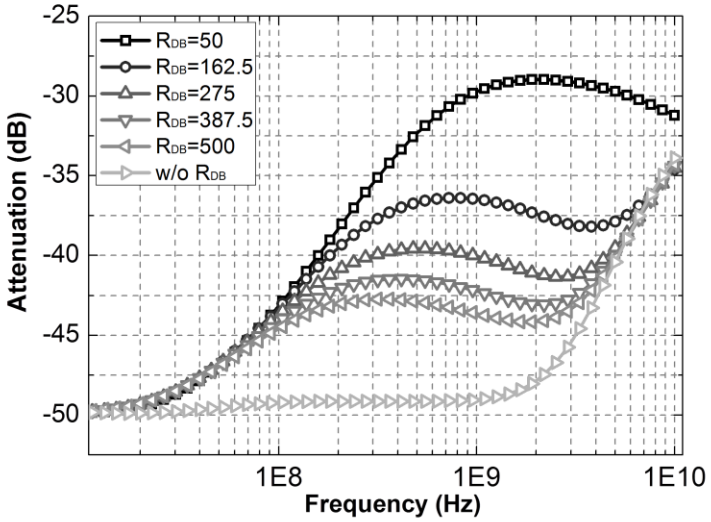


Figure 2.15 Frequency responses of attenuators with different R_{DB} values at their maximum attenuation settings

maximum attenuation and the bandwidth of the attenuator. Therefore, the R_{DB} value should be carefully chosen to have cutoff frequency low enough to meet the desired bandwidth.

Another frequency-related factor is linearity. Previous research [11], [32] indicates that gate coupling is very effective at a higher frequency; body coupling is likewise frequency dependent. Figure 2.16 presents the IP_{1dB} simulation results of the final design at different frequencies. The worst-case IP_{1dB} is 6.4 dBm at 700 MHz, 8 dBm at 1 GHz, 8.4 dBm at 2 GHz, and 9 dBm at 3.7

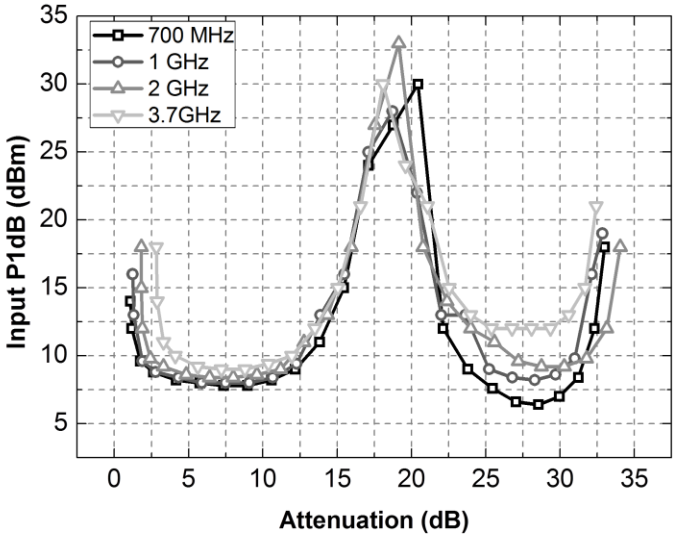


Figure 2.16 Simulated IP_{1dB} at different frequencies

GHz. The figure shows that linearity improves as frequency increases; this trend is even more apparent in higher attenuation region II, in which improvement occurs mainly due to the effect of coupling.

2.4 ATTENUATOR IMPLEMENTATION AND MEASUREMENTS

This section demonstrates a CMOS variable attenuator design using the adaptive bootstrapped body biasing techniques described above and optimized for WCDMA applications. The attenuator core is a 3-stage π-type network, illustrated in Figure 2.17, and the complete voltage controlled attenuator schematic diagram is shown in Figure 2.18. While in a previous work [11], three sets of control and matching blocks and four series transistors are used to improve linearity, only one control, one matching block, and three series transistors are used in the proposed design. The reason for selecting this topology is to show that an originally non-linear attenuator can have a better power handling capability with the proposed linearization

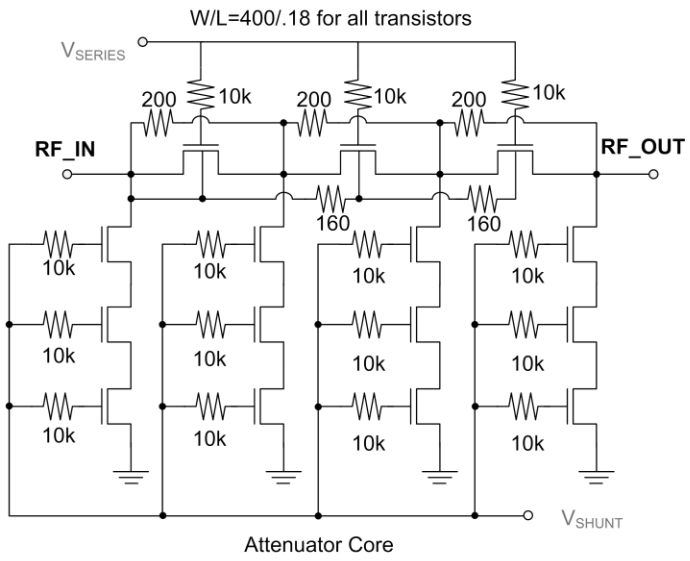


Figure 2.17 The schematic diagram of the proposed attenuator core

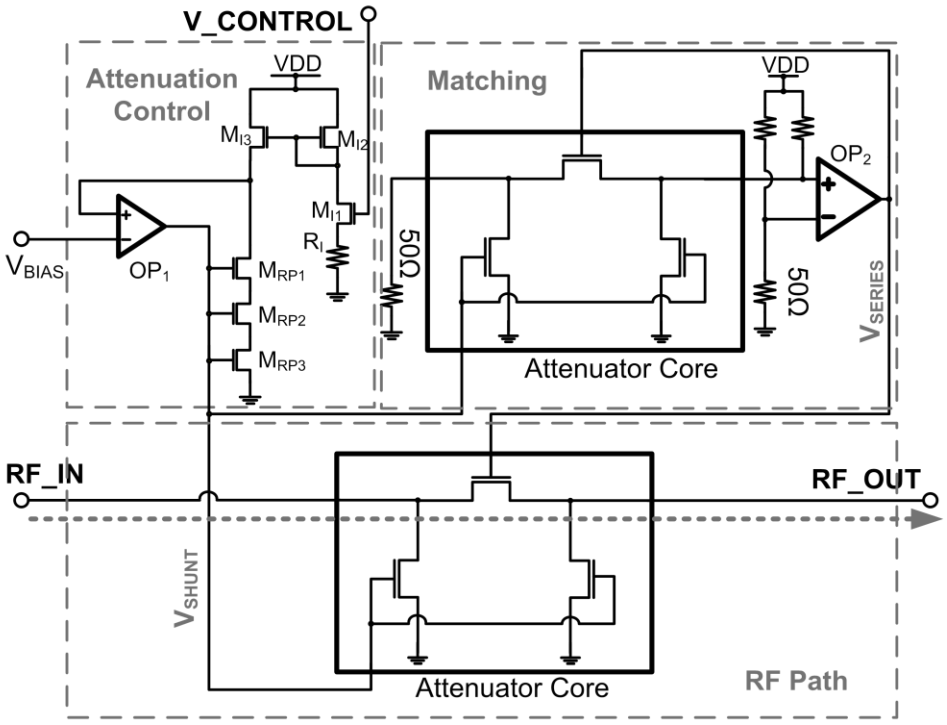


Figure 2.18 The schematic diagram of the entire variable attenuator, with control and matching

technique.

In addition, the topology has a better linear-in-dB control nature and is not very sensitive to the temperature variation [12], as illustrated in Figure 2.19. The resistances of shunt branches

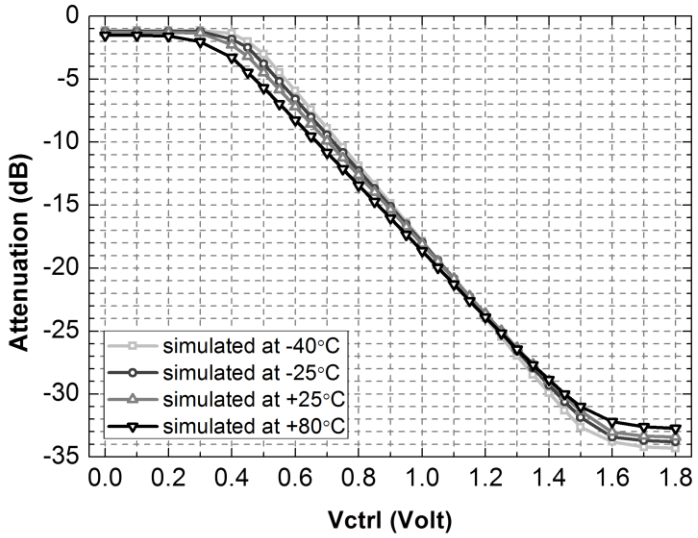


Figure 2.19 Simulated attenuation versus Vctrl curves of the proposed attenuator at different temperatures and at 1.95 GHz. All the bias voltages are set constant at every temperature. The maximum attenuation and the control slope changes 1.5 dB and 12%, respectively from -40°C to 80°C

in this attenuator are not directly controlled by an external signal but through a current source and a feedback loop. $M_{I1,}$ M_{I2}, M_{I3}, and R_I convert an input control voltage to a current signal, and feed it to M_{RP1}, M_{RP2}, and M_{RP3}, which replicates the shunt branches in the attenuator core. An OP-AMP (OP_1) locks the voltage drop across the shunt branch to a reference value (V_{BIAS}) by controlling the gate bias (V_{SHUNT}) of M_{RP1}, M_{RP2}, and M_{RP3}. As more current flows into the replicated shunt branch, the generated V_{SHUNT} signal reduces the channel resistance of the shunt transistors in the attenuator core. Meanwhile, the matching block senses a drop in input impedance, thus lowering the gate bias of the series transistors accordingly to ensure proper

matching. The attenuation value is decibel linear to the control voltage, and the slope of the control curve is determined by the V_{BIAS}.

The proposed design has been fabricated in a 0.18-μm RF CMOS technology with triple-well devices. As shown in Figure 2.20, the die size of the attenuator is 750 × 375 μm^2, including I/O pads. Two biases (V_{B1} and V_{B2}) were assigned externally to the Op-amps and are set to the values (0.5 V and 0.1 V) used in the simulation. The die was mounted on a printed circuit board (PCB) for a chip-on-board (COB) measurement as shown in Figure 2.21. As demonstrated in

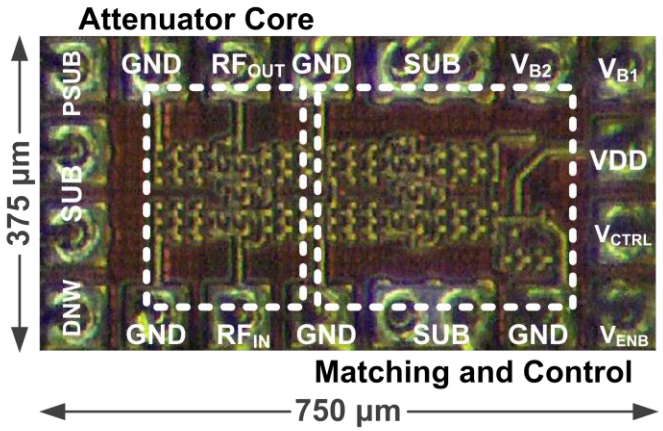


Figure 2.20 Microphotograph of the attenuator

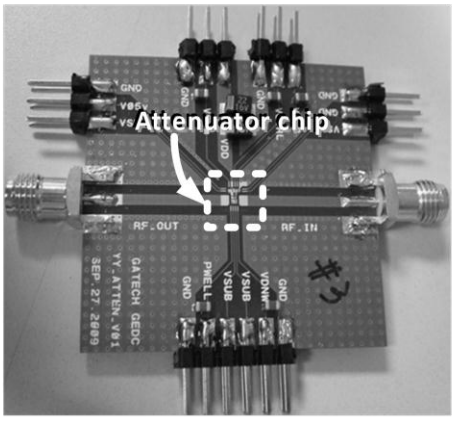


Figure 2.21 Testing PCB board with the attenuator chip

Figure 2.22, while the parasitic inductance from the down-bonding wires has little influence on the overall attenuation range, it increases the insertion phase variation of the attenuator and therefore should be minimized.

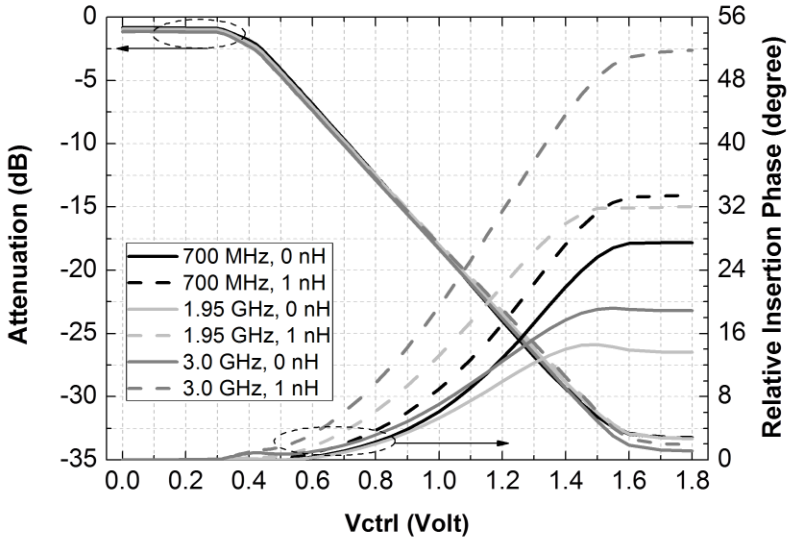


Figure 2.22 Simulated attenuation and insertion phase versus Vctrl curves of the proposed attenuator at different frequencies. Inductors are put between each shunt branches and the ground to simulate the parasitic effect of the down-bonding wires. With a perfect ground (0 nH, solid lines), the attenuator will have the largest insertion phase variation at 700 MHz, but with 1 nH parasitic inductance (dashed lines), the insertion phase variation at higher frequencies will be increased dramatically.

The Linearity performance and linear-in-dB controllability were measured with an Agilent E4433B Signal Generator, an Agilent E4417A Power Meter, and an Agilent E4440A Spectrum Analyzer along with two Agilent E9300A AVG Power Sensors and Megaphase cables. The S-parameters were measured with an Agilent N5230A Network Analyzer. An external control signal was applied to the variable attenuator, and the relationship between the control voltage and the attenuation is shown in Figure 2.23. The curve was measured at 1.95 GHz (the

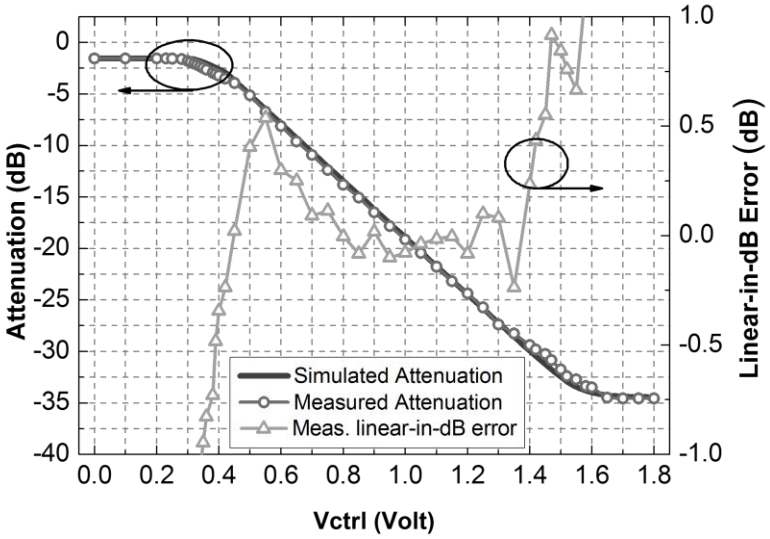


Figure 2.23 Measured and simulated linear-in-dB control curves, and measured linear-in-dB error at 1.95 GHz

center frequency of WCDMA band I) and with an input power of -5 dBm. Most of the measured gains comply with the simulation results except those in the transition corners. It is because in each corner, either series or shunt transistors are biased near the boundary cut-off and triode region, and the model may not be accurate enough to predict the actual attenuation. Measured maximum and minimum attenuations at 1.95 GHz are -34.6 dB and -1.6 dB, respectively. A fitted gain control line was calculated based on the measurement results, and its slope is -27 dB/V. The error from the measured attenuation to the line, referred to as a linear-in-dB control error, is also shown in the same figure. The error over a 30 dB tuning range is less than ±1 dB, which indicates good linear-in-dB controllability.

Figure 2.24 illustrates the frequency response of S_{21} at different control voltages. The high-pass response is most obvious at the highest attenuation settings. Thus, this setting is used to determine the lower cut-off frequency of the entire attenuator. The higher corner frequency,

however, is determined at the lowest attenuation setup. According to the measurement results, this attenuator can operate from 400 MHz to 3.7 GHz with a worst-case attenuation flatness of 2.6 dB at all attenuation settings. The minimum insertion loss (IL) variation is less than 2.1 dB from DC to 3.7 GHz and less than 2 dB from 400 MHz to 3.7 GHz. The measured insertion phase variation at different attenuation settings and frequencies are plotted in Figure 2.25. As

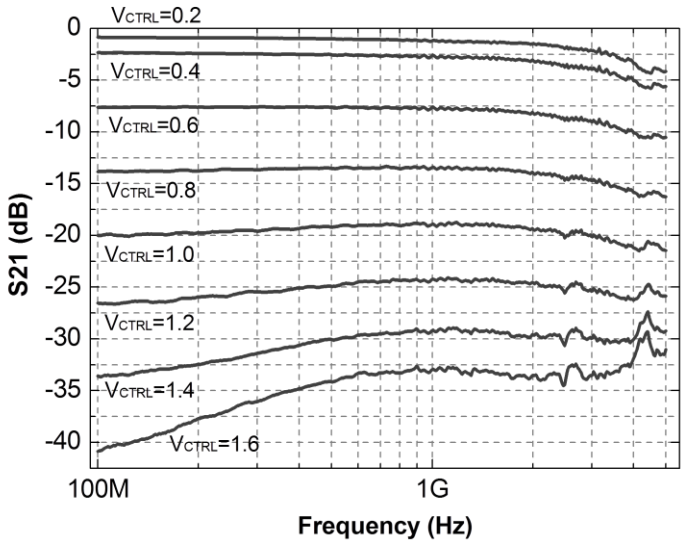


Figure 2.24 Measured frequency response of the attenuator at different control voltages

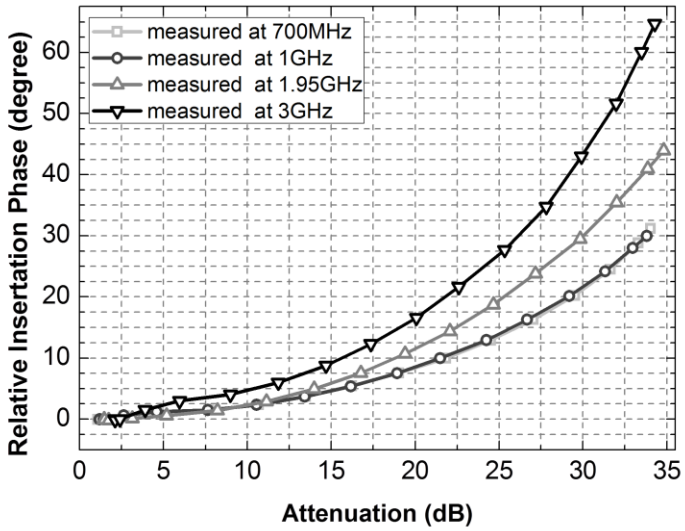


Figure 2.25 Measured and simulated phase variation at different attenuation settings and frequencies

expected, the down-bonding parasitics increase the phase variation of the attenuator as comparing to the simulated insertion phase variation with ideal ground in Figure 2.22.

The input and output return loss (S_{11} and S_{22}) at different frequencies and control voltages are plotted in Figure 2.26. The asymmetrical body connections cause the variations between S_{11} and S_{22}. The worst-case return loss occurs at the first knee point of the control curve for the attenuator. The worst-case S_{11} and S_{22} are -9.1 dB and -9.6 dB, respectively. The simulated

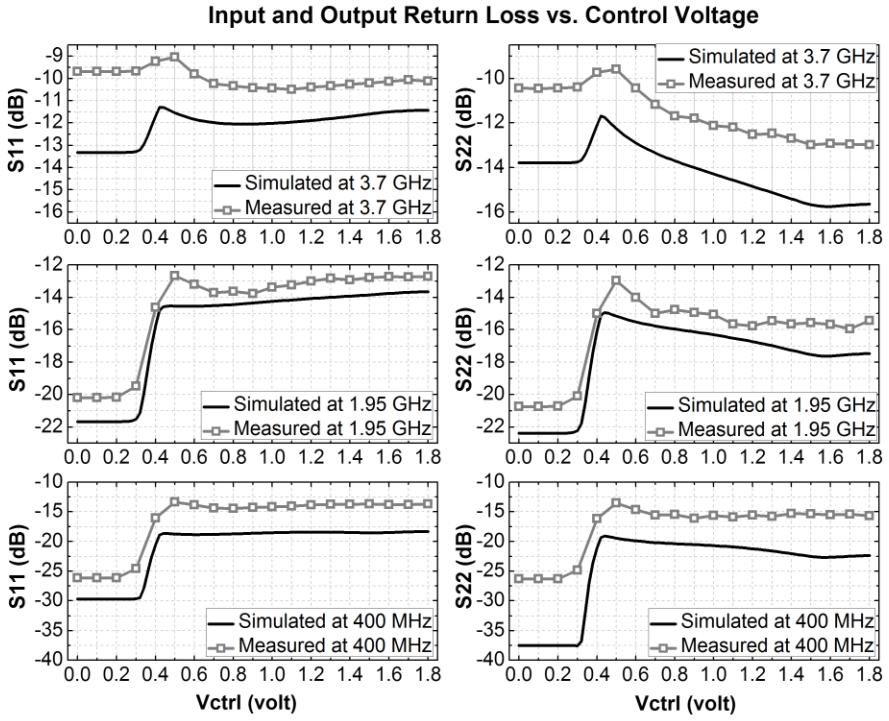


Figure 2.26 Input and output return loss versus the control signal at different frequencies

results are closest to the measurements at 1.95 GHz since the 50-Ω transmission lines on the PCB board are designed for this frequency.

Figure 2.27 plots the attenuation values versus the input power at different attenuation settings and Figure 2.28 shows the IP_{1dB} at different attenuations. A bottleneck of power

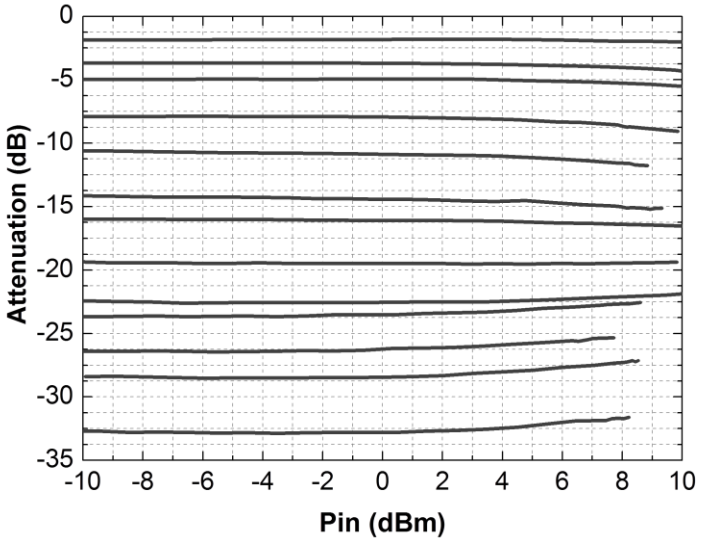


Figure 2.27 Measured attenuation versus input power at different control voltages and at 1.95 GHz

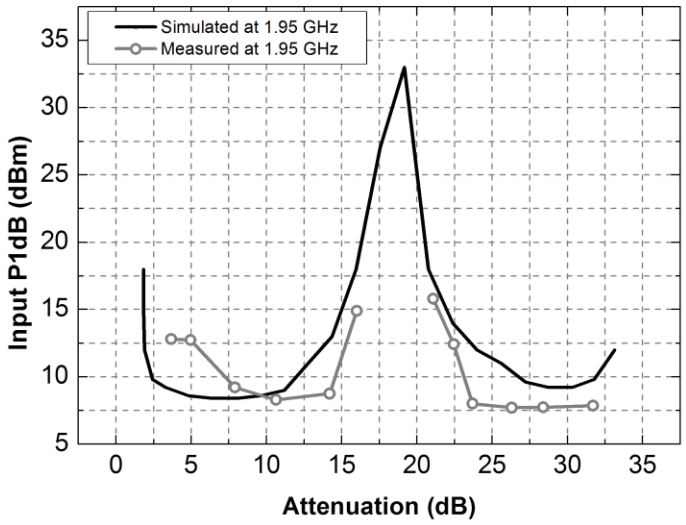


Figure 2.28 Simulated and measured IP_{1dB} at different attenuation value and at 1.95 GHz

handling takes place at higher attenuation settings. While the measured worst-case IP_{1dB} is better than 7.5 dBm at 1.95 GHz, it is 8.4 dBm in simulation. There is a gap between the two measurement sections because the gain compression at mid-attenuation is a lot lower than 1 dB

even at 15 dBm input power.

As mentioned earlier, because IP_{1dB} points are affected by voltage coupling at the gate and body terminals, they are influenced by the frequency. Gate and body coupling are both better at higher frequencies and so does the linearity performance. The measurements show that IP_{1dB} points are greater than 6 dBm at 700 MHz, greater than 7 dBm at 1 GHz, and greater than 7.5 dBm at 1.95GHz where the attenuator is been optimized. The measured values of IP_{1dB} at different signal frequencies and in the high attenuation region are plotted in Figure 2.29.

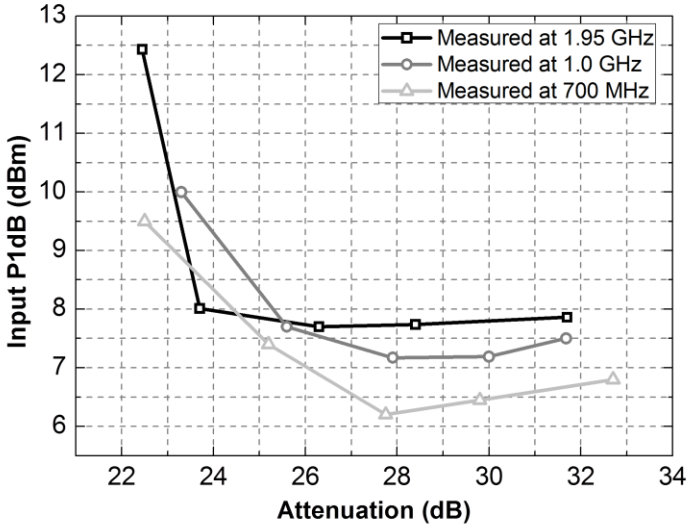


Figure 2.29 Measured IP_{1dB} in the higher attenuation region and at different frequencies

Figure 2.30 shows the level of intermodulation distortion effects of the attenuator in terms of input-referred third-order intercept point (IIP_3). The input power for the measurements is -8 dBm for low attenuation settings and -3 dBm for high attenuation settings. Measured IIP_3 points at different attenuation values exhibit a trend similar to those of the IP_{1dB}. The worst-case IIP_3 tested with two tones at 1948.5 MHz and 1951.5 MHz is better than 17 dBm. Both IP_{1dB} and IIP_3 are the best among similar CMOS designs. The specification of the proposed attenuator is

summarized and compared with previous designs in Table 2.1.

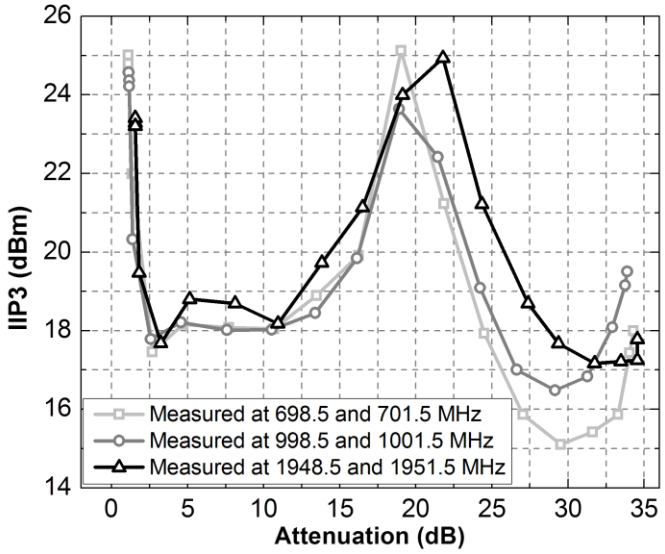


Figure 2.30 Measured IIP_3 at different attenuation values and at different frequencies

Table 2.1 Comparison Between CMOS Attenuators

References	Kaunisto [2]	Dogan [1]	This work
Technology	0.8-μm CMOS	0.13-μm CMOS	0.18-μm CMOS
Chip Area	850 × 1850 μm^2	700 × 1000 μm^2	750 × 375 μm^2
Frequency	DC-900 MHz	DC-2.5 GHz	400 MHz-3.7 GHz (with linear-in-dB control curve)
Minimum Attenuation	3.3 dB	0.9-3.5 dB	0.96~2.91 dB
Max. Attenuation Range	28 dB	42 dB	33 dB (30 dB with a ±1 dB linear-in-dB error)
Return Loss	>-12 dB	>-8.2 dB	>-9 dB
Attenuation flatness	N/A	2.6 dB (DC-2.5 GHz)	2.6 dB (400 MHz-3.7 GHz)
Incremental Noise	< 1 dB	1 dB	1 dB
Worst-case IIP_3	N/A	~ 10 dBm (at 1 GHz)	> 17 dBm (at 1.95 GHz) > 16.5 dBm (at 1 GHz) > 15 dBm (at 700 MHz)
1dB Compression point	5 dBm	2.5 dBm	> 7.5 dBm (at 1.95GHz) > 7 dBm (at 1GHz) > 6 dBm (at 700 MHz)

CHAPTER 3

A HIGHLY LINEAR VARIABLE GAIN AMPLIFIER FOR ANALOG PREDISTORTION SYSTEMS

3.1 INTRODUCTION

A new RF VGA topology based on aforementioned attenuator is presented in this chapter. Through the detail analysis and experiment results, it demonstrates a much better capability of handling higher input power, having a relatively wide bandwidth, smaller size and a continuous control curve than ant conventional CMOS RF VGA. Its key design blocks will be analyzed in section II, while the measurement results will be shown and compared with other CMOS work in section III.

3.2 RF VGA TOPOLOGY AND KEY DESIGN BLOCKS

The pros and cons of different VGA topologies have been well analyzed previously in chapter 1. Although those receiver VGA topologies are unable to meet all the requirements to be used as predistortion circuit, the analysis of heir characteristics gives a direction when designing an appropriate topology for VGAs in an analog-predistortion PA system.

A simple analysis of the system in Figure 1.7 can help specify the exact features this VGA requires. First, the VGA in Figure 1.7 is put outside the detection and comparison loop and a linear-in-dB power detector is employed to detect the gain error of the PA and to generate the

gain control signal in the analog domain. This topology reduces the settling time and avoids the use of accurate/high-speed A/D converters (which reduces the design complexity and the power consumption of the system); but requires an analog-control VGA with a linear-in-dB gain control curve. In addition, the VGA is placed after the up-converter to relax the linearity requirement of the mixer in the up-converter. Therefore, the input-signal of this VGA is at the RF frequency (up to 2 GHz depends on which WCDMA band is selected), and the input power will be close to 0 dBm depends on the gain of the PA and the RF VGA itself. These make the bandwidth and linearity primary concerns when designing such RF VGA.

Based on the analysis in [15]-[16], [23], a smaller transconductance and load impedance variation for the amplifier stage generally ensure it to stay near the optimum bias point, thereby allowing the RF VGA to have better linearity. On the other hand, a smaller parasitic capacitance from a tunable load with smaller and fewer transistors is preferable for wideband operation. Therefore, an ideal linear-in-dB controlled RF VGA topology will be one that utilizes active circuits which stay near their optimized bias condition and drive simple and fixed loads with low parasitics.

Among the traditional topologies, pre-attenuated RF VGAs have these features and show excellent linearity and bandwidth [23], making them potential candidates for signal predistortion in the mentioned PA system. In such a type of RF VGA, variable attenuators are put in the input to change the signal strength, while a second variable- or fixed- gain stage is used to provide sufficient gain. Since the input attenuator carries most of the burden of gain-tuning and reduces the input power, the amplifier stage is allowed to have a smaller gain-tuning range and handles lower input power. A smaller gain-tuning range reduces the DC bias variation of the amplifier, while a lower input power relaxes the amplifier's voltage swing requirement. Both of these help

increase the overall linearity of the RF VGA. However, a serious problem in attaining good linearity of a pre-attenuated RF VGA is its poor noise figure resulting from the pre-attenuation. Although noise specification is relatively loose for transmitters, a pre-attenuated RF VGA may contribute too much noise especially when operating at its lowest gain settings. Except for noise figure, the attenuator based RF VGA has most of the features a predistorter requires.

The idea of the proposed RF VGA is based on the pre-attenuated RF VGA topology, and the simplified schematic diagram is illustrated in Figure 3.1. Instead of using an input attenuator,

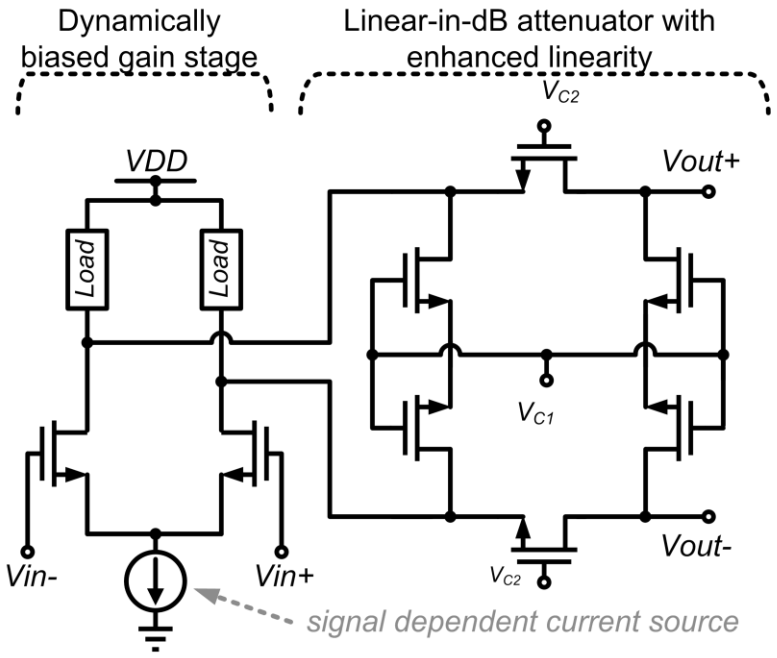


Figure 3.1 Proposed post-attenuated RF VGA topology

the gain of the proposed RF VGA is controlled by a highly linear, fixed-input-impedance attenuator that also works as a part of the load to the gain stage. The input impedance of the attenuator should remain relatively constant, so that the amplifier stage can always drive the loading impedance it's been optimized for. The attenuator also takes the major responsibility for

tuning the overall gain, thereby allowing the amplifier stage to have a constant DC bias which results in a better linearity.

Different from the pre-attenuated RF VGA, a pre-amplified topology will give the RF VGA a better noise performance. This can be demonstrated with the noise factor equation for cascade stages [36]:

$$F_{RFVGA} = F_{GAIN} + \frac{F_{TUNE} - 1}{G_{GAIN}} \quad (3.1),$$

where F_{RFVGA} is the overall noise factor of the RF VGA, F_{GAIN} and F_{TUNE} the noise factor of the gain and tuning stage respectively, and G_{GAIN} the gain of the gain stage. Because the influence of the noise from the second-stage attenuator (F_{TUNE}) is reduced by the gain of the first-stage amplifier (G_{GAIN}), this RF VGA topology not only has the advantage of linearity and bandwidth inherited from attenuator-based RF VGA, but also a better noise figure than a pre-attenuated RF VGA.

However, there are two challenges of implementing such a RF VGA in CMOS technology. One is to improve the power handling capability of a differential amplifier and the other is to design a highly linear attenuator with high input impedance. These two circuits along with their design issues will be discussed thoroughly in this section.

3.2.1 Fixed Gain Amplifier with Dynamic Current Bias

The amplifier stage determines the gain and noise figure, and has critical influence on the linearity of the RF VGA. Inductive loads are commonly used in RF amplifiers both to expand the output AC voltage swing and the bandwidth. However, inductors are bulky, and the chip size of a differential RF VGA using two inductors will be unreasonably large. Therefore, instead of using inductors, the amplifier in the proposed RF VGA adapts the concept of dynamic current

boost [37] in combined with a self-biased differential pair to extend the gain flatness to a higher input power.

Figure 3.2 shows the schematic diagram of the proposed amplifier stage. The dynamic current bias of this amplifier consists of a reference DC current source and an input power

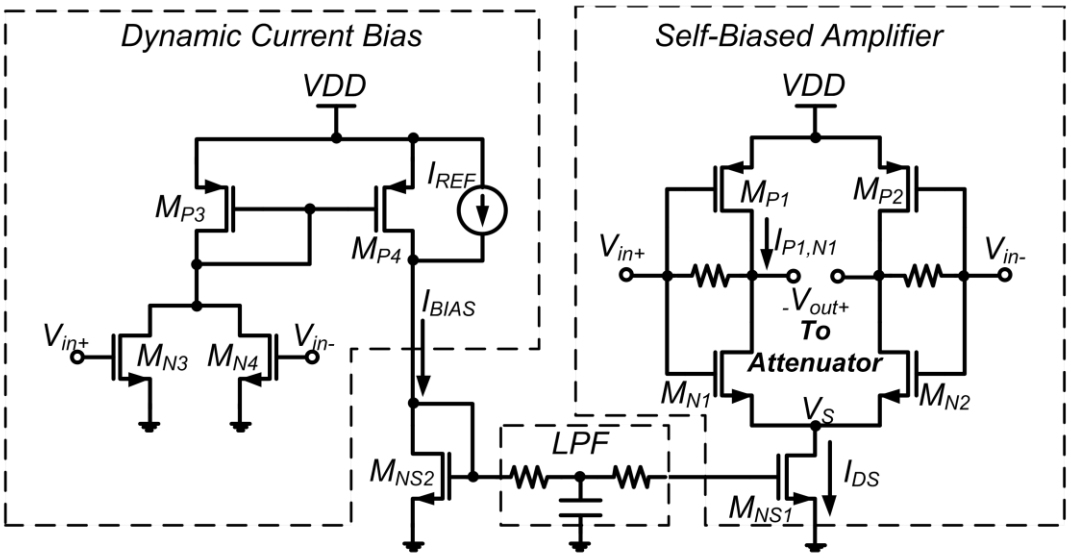


Figure 3.2 The schematic diagram of the gain stage with dynamic current bias

detector. The power detector generates a dynamic bias current with the magnitude determined by the input power. The low pass filter (LPF) at the output of the dynamic bias circuit allows only the low-frequency components to pass though, dynamically adjusting the gate voltage and the drain current of M_{NS1}. The transconductance (g_m) of M_{N1} and M_{P1} can be calculated based on equation [36]:

$$g_m = \sqrt{2\mu_{p,n} C_{ox} (W/L) I_{P1,N1}} \qquad (3.2),$$

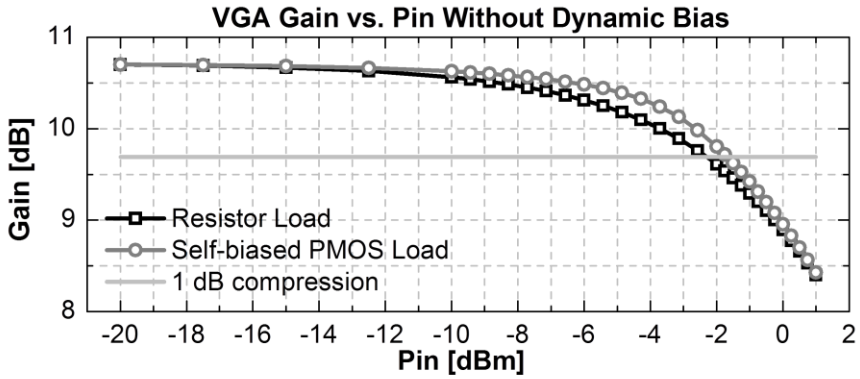
where $\mu_{p,n}$ is the mobility of the charge carrier of p- or n- MOS, C_{OX} is the gate oxide capacitance per unit area, and W/L is the aspect ratio of the transistor. In addition, $I_{P1,N1}$ is the bias current passing through M_{P1} and M_{N1}, and the amount is controlled by M_{NS1}. Therefore, when the input power increases, a carefully designed power detector can properly increase the current of M_{NS1} and hence the g_m of the amplifier to compensate the gain compression due to a large input signal.

Since the dynamic current bias only supplies currents at a higher input power, the transistor M_{N3} and M_{N4} are biased between class B and class C. When the input voltage swing exceeds a designated level, M_{N3} and M_{N4} will convert it to current signals. These currents are added together at M_{P3}, and the magnitude of the overall current reflects the input power. M_{P4} then copies the drain current of M_{P3} and adds to a DC bias current I_{REF} at M_{NS2}. Therefore, the drain current of M_{NS2} contains several different frequency components including one at DC (I_{REF}), one at the frequency of the signal envelope, and one at the carrier frequency. Because nonlinear effects such as AM-AM or AM-PM errors are caused by the amplitude-dependent gain response, the envelope of the RF signal can be used to determine whether to activate the gain compensation. To extract the envelope information and filter out high frequency components, the cutoff frequency of the LPF is set slightly higher than the envelope bandwidth. The output of the LPF is then connected to the gate of M_{NS1}, controlling its drain currents to compensate for the gain compression.

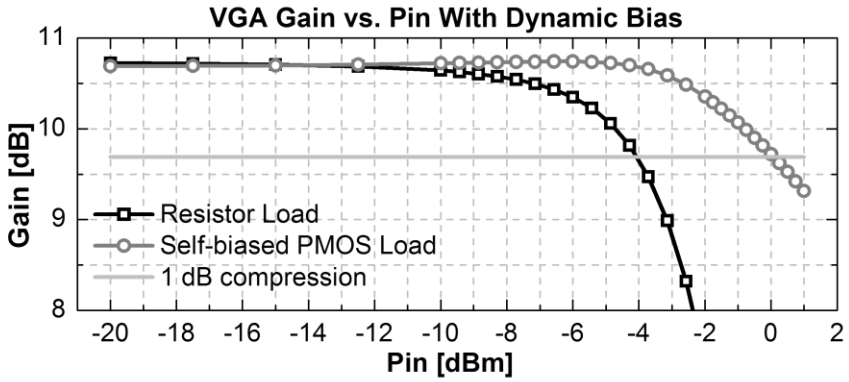
However, this dynamic current biasing only works for certain amplifier topologies and might degrade the linearity of an amplifier with inappropriate loads. Different from [37], the proposed RF VGA design does not use inductors. This means the dynamic current will change the common mode voltage at the output of an amplifier, and thereby changing the operation region of its transistors. To examine how the voltage change affects the linearity in different

amplifier topologies, we compared the performance between a resistively loaded differential pair to a self-biased one, before and after initiating the dynamic current supply.

As demonstrated in Figure 3.3(a), a differential amplifier with self-biased PMOS loads has similar P_{1dB} compared to one with resistor loads, when they are both biased with a DC current source. However, if the bias current increases dynamically with the input power, self-biased PMOS loads can give better linearity to the amplifier while resistor loads degrade its linearity, as shown in Figure 3.3(b). The ability to keep a constant output common mode voltage can explain



(a)



(b)

Figure 3.3 Gain versus input power of two amplifiers simulated with 1.95 GHz input signals. The results in (a) and (b) shows the gain flatness while both amplifiers are biased with DC current and dynamic current source, respectively.

this difference. Referring to Figure 3.2, the output common mode voltage $V_{OUT,CM}$ of a self-biased amplifier can be calculated to be:

$$V_{OUT,CM} = V_{DD} - |V_{TP}| - \sqrt{\frac{I_{DS}}{\mu_p C_{OX}\left(\frac{W}{L}\right)_p}} \quad (3.3),$$

where μ_p is the mobility, V_{TP} the threshold voltage of M_{P1} or M_{P2}. In addition, I_{DS} is the total bias current of the amplifier. The square root relationship between $V_{OUT,CM}$ and I_{DS} in (3) reduces the output common mode voltage drop of a self-biased amplifier when a higher drain current is applied. On the contrary, the output common mode voltage of an amplifier with resistor loads has a linear relationship with its bias current. Its output voltage drops quickly when the dynamic current is high, thereby driving the transistors into the triode region.

Simulation results that compare the bias voltage variation between amplifiers with two different types of load are shown in Figure 3.4. The amount of current used to compensate for

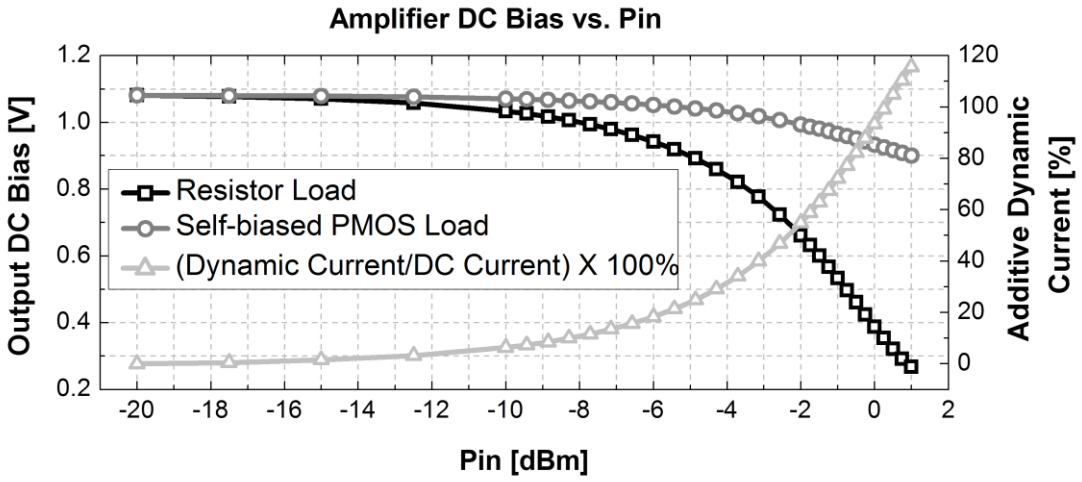


Figure 3.4 Output common mode voltage of different amplifiers with and without dynamic current source (simulated with 1.95 GHz input signal).

the gain variation of a self-biased PMOS load amplifier lowers its output common mode voltage by 8% at -2 dBm input power, but the common mode voltage of resistor-load amplifier drops 38% with the same amount of current. The output voltage of a resistively loaded amplifier will be too low to keep all the transistors in the saturation region at this input power level. Hence the dynamic current does not help but rather degrades the linearity of a resistively loaded amplifier. Hence a self-biased amplifier is selected as the gain stage in this RF VGA design, and a linear attenuator will be connected to its output to tune the overall gain while maintaining linearity.

3.2.2 Highly Linear Gain Tuning Attenuator

The variable attenuator in the proposed RF VGA employs the multi-stack series transistors and the bootstrapped body biasing technique [38], to enhance the overall linearity of the RF VGA. Its schematic diagram is shown in Figure 3.5. As addressed in the reported literature [11], [27], [38]-[39], the non-linear responses of an attenuator are caused by the impedance variation of its transistors and are especially serious when the control voltage is close to the threshold voltage (V_{TH}) of the transistor. Comparing to a 50-Ω matched attenuator, the attenuator designed with high input impedance has much significant gain variation because the control voltage will be set closer to V_{TH} to get a higher channel resistance. Using more transistors in a stack and a smaller bootstrapped body biasing resistor (R_{DB}) could still allow the attenuator in the proposed RF VGA to have enough linearity, but at the cost of bandwidth.

To improve the gain flatness in the lower attenuation region, triple-stacked transistors are used in each shunt branch of the proposed attenuator, making it a total of six transistors to carry the overall differential voltage swing. This number is selected to get the best linearity and an upper-cutoff frequency that covers most of the WCDMA uplink. On the other hand, utilizing a smaller body biasing resistance (R_{DB}) improves the linearity in the high attenuation region, but

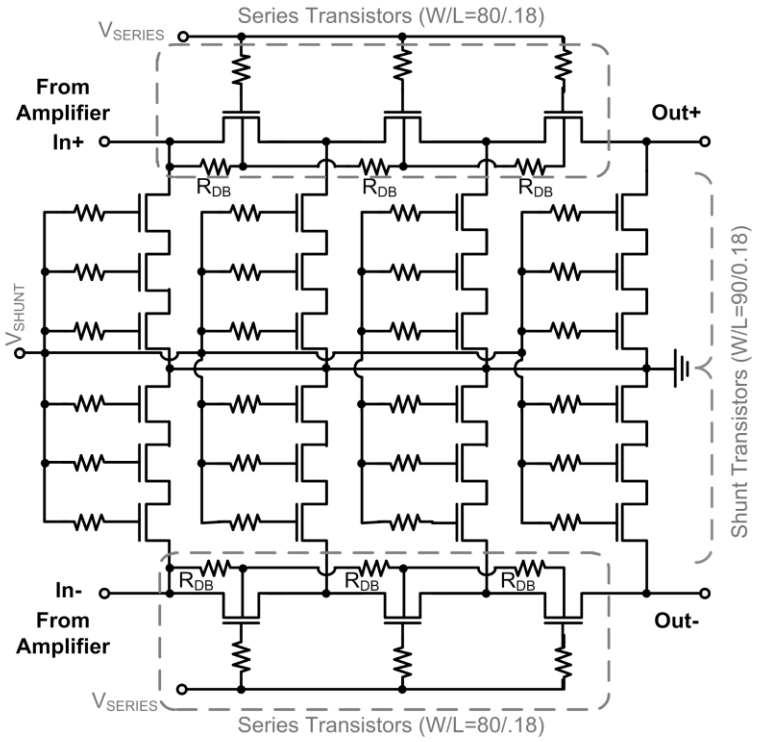


Figure 3.5 Two attenuators with bootstrapped body bias are connected differentially

results in a higher lower-cutoff frequency [27]. Hence a much narrower bandwidth is expected if an attenuator is designed to have both high input impedance and uses a very small body biasing resistance to improve its linearity.

However, designing a whole RF VGA is different from designing an attenuator alone. Figure 3.6 shows the gain versus input power of a π-type attenuator without body bias R_{DB}, and at different gain settings. The gain responses at a higher input power have two different directions of variation. In the lower attenuation region, the gain compresses as the input power goes high, but the gain increases with the input power in the high attenuation region. While we try use multi-stack transistors to alleviate the compression in the low attenuation region, the increasing gain in the higher attenuation region can be used to compensate for the decreasing

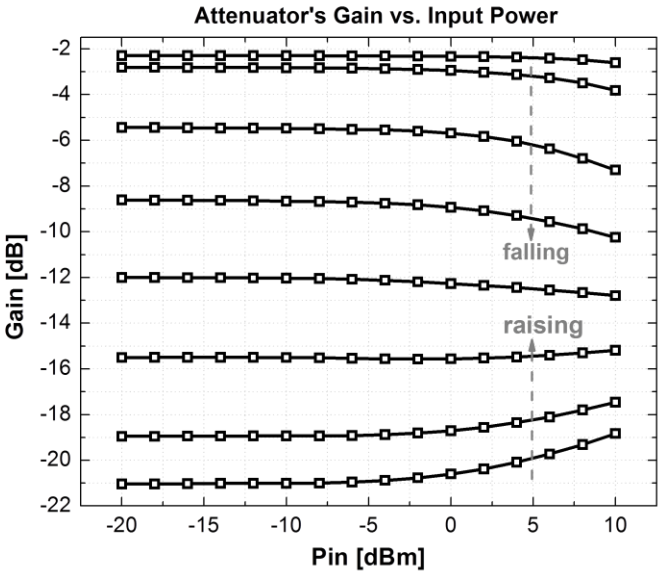


Figure 3.6 Attenuator's gain versus input power at different gain settings, simulated at 1.95 GHz.

gain of the amplifier stage, and benefits the overall linearity of the RF VGA. This allows us to use a larger R_{DB} to slightly push the gain increasing point to a higher input power to avoid gain peaking at a mid-level input power, and solves linearity-bandwidth dilemma.

Simulations are performed to find the R_{DB} value that shows reasonable trade-off between lower corner-frequency and linearity of the RF VGA. As illustrated in Figure 3.7 and 3.8, decreasing R_{DB} value reduces the gain peaking at a higher input power but also reduces the bandwidth. Figure 3.9 plots the simulated results of these trade-offs. The lower corner- frequency drops rapidly in the beginning but reaches its limit when R_{DB} is greater than 200 Ω, while the peaking reduction gradually reaches its limit when R_{DB} is greater than 200 Ω. Therefore, the R_{DB} value of this design is chosen near 200 Ω to both achieve a good linearity and a sufficient bandwidth.

The complete schematic diagram of the proposed RF VGA is illustrated in Figure 3.10. The

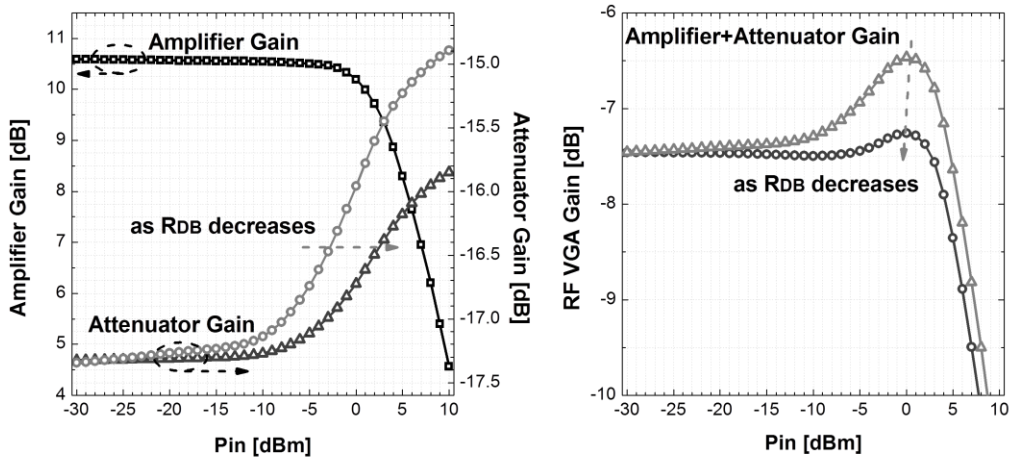


Figure 3.7 How the R_{DB} value affects the RF VGA gain flatness

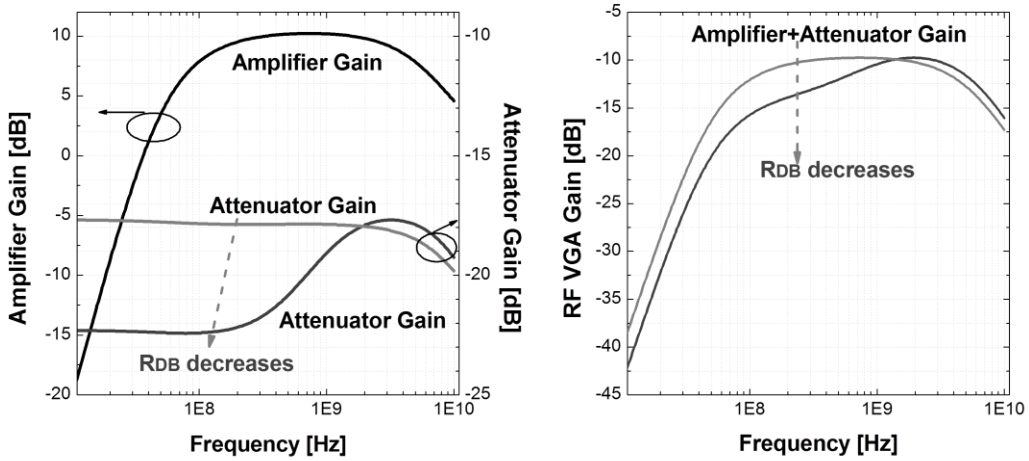


Figure 3.8 How the R_{DB} value affects the RF VGA frequency response

control circuitry of the attenuator is used to closely approximate a linear-in-dB curve [10], resulting in an RF VGA that has a similar control curve. The slope of the curve can be adjusted by V_{REF}.

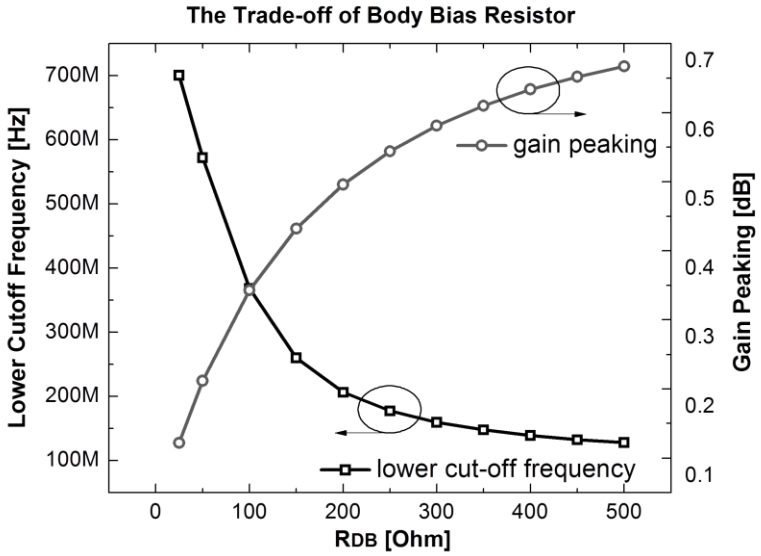


Figure 3.9 Lower-cutoff frequency and gain peaking of the overall RF VGA with different values of R_{DB}

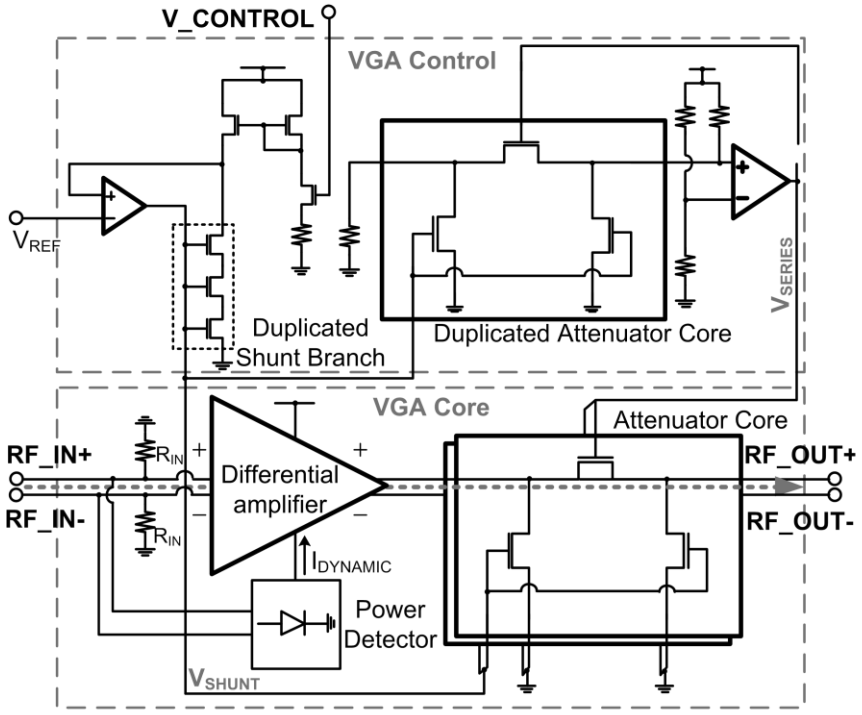


Figure 3.10 The completed schematic diagram of the RF VGA

3.3 MEASUREMENT RESULTS

The proposed RF VGA has been fabricated in a standard 0.18-μm CMOS technology, and the die was mounted on a printed circuit board for a chip-on-board measurement. Its measurement buffer was fabricated in an independent die, so that the characteristics could be measured and de-embedded. The chip microphotograph is shown in Figure 3.11, and the overall active area of the RF VGA is around 400×270 μm^2.

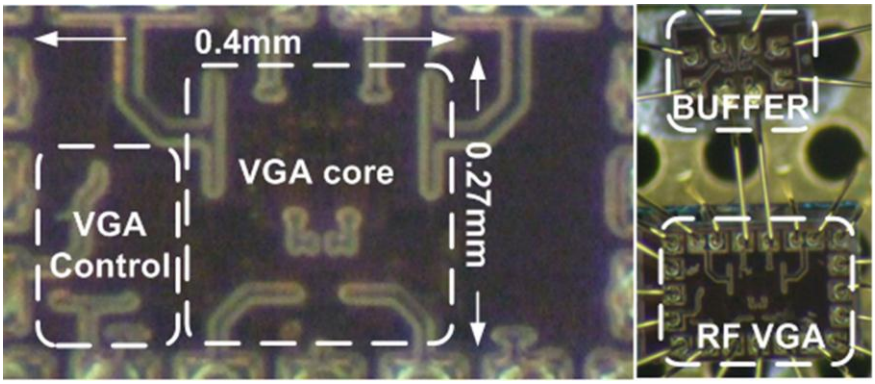


Figure 3.11 Photograph of the chip and measurement buffer

Figure 3.12 shows the frequency responses of the RF VGA. Its 3-dB bandwidth at the maximum gain setting is from 30 MHz to 2.2 GHz, but the tilted frequency response at the minimum gain setting has a much higher lower corner-frequency. To keep the in-band gain flatness smaller than 3-dB at all gain settings, the actual operation frequency of the RF VGA should be limited to 380 MHz to 2.2 GHz. This bandwidth is enough to cover most of the WCDMA uplink. The RFVGA has a maximum gain of 13.5 dB and a minimum gain of -13.5 dB within the frequency band.

Figure 3.13(a) and 3.13(b) plot the measured and simulated gain versus control curves at 850 MHz and 1950 MHz respectively. The measured maximum gain is well matched to the

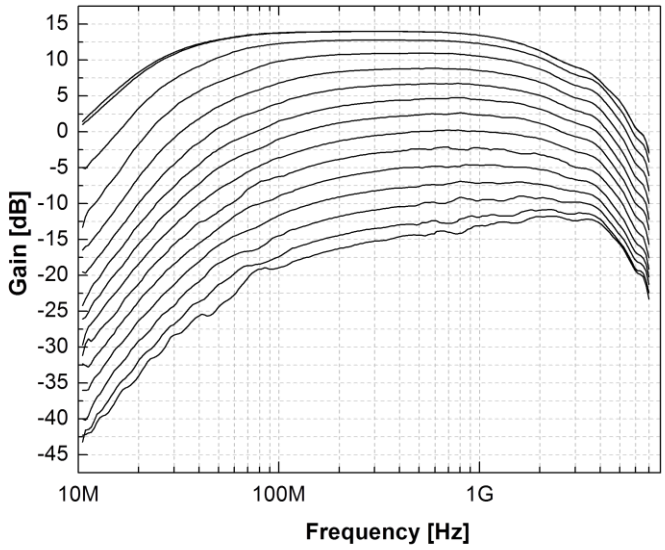
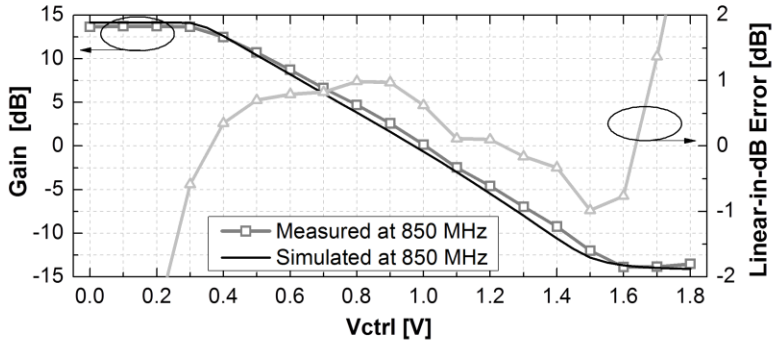
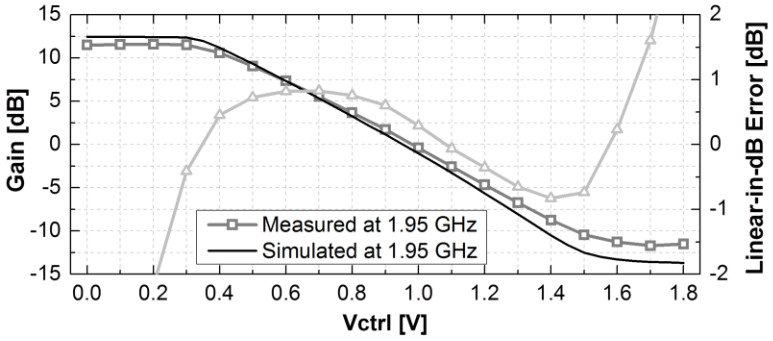


Figure 3.12 Measured frequency responses of the RF VGA at different gain settings



(a)



(b)

Figure 3.13 Measured and simulated gain versus the control voltage of the RF VGA at (a) 850 MHz

simulated results at 850 MHz, but has about 1 dB difference at 1950 MHz. Besides, the measured minimum gain is slightly higher than the simulated results. The gain deviation is mainly due to the parasitic inductance of ground-bonding wires, which increases the impedance to ground at higher frequency and thus reducing the attenuation.

The RF VGA is also designed to have a linear-in-dB control curve. To demonstrate how good the approximation is, a fit to the gain-control line is calculated based on the measurement data. The differences between each measured gain to the fitted line (known as linear-in-dB error) are shown in the same graph. The linear-in-dB error of the RF VGA is less than ±1 dB over all the effective control range, which is from 13.5 dB to -13.5 dB at 850 MHz and from 11.5 dB to -11.5 dB at 1950 MHz.

Figure 3.14 gives the input P_{1dB} results measured at different gain settings. The worst-case input P_{1dB} is -5 dBm at 850 MHz and -3.6 dBm at 1950 MHz. Two-tone measurements are also performed to show the intermodulation distortion of this RF VGA. Measured IIP_3 at each gain

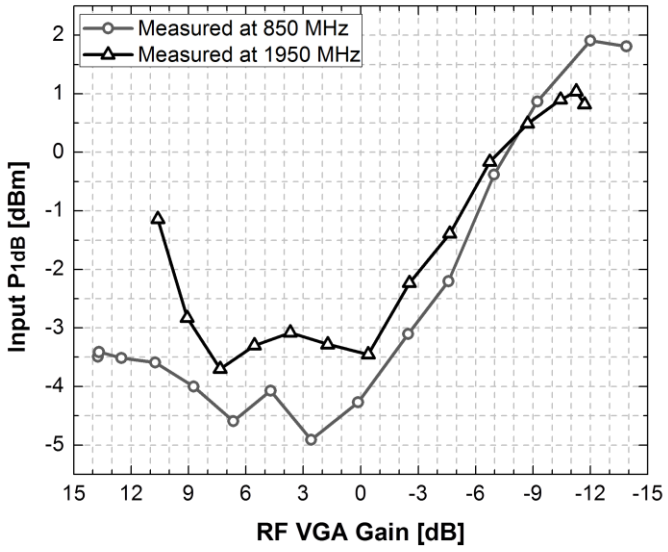


Figure 3.14 Measured gain and noise figure of the RF VGA versus the control voltage

settings are plotted in Figure 3.15 (a), while Figure 3.15 (b) gives the measured signal power and 3rd harmonic at the most-nonlinear gain setting (5.5dB gain, Vctrl=0.7). The tone spacing is

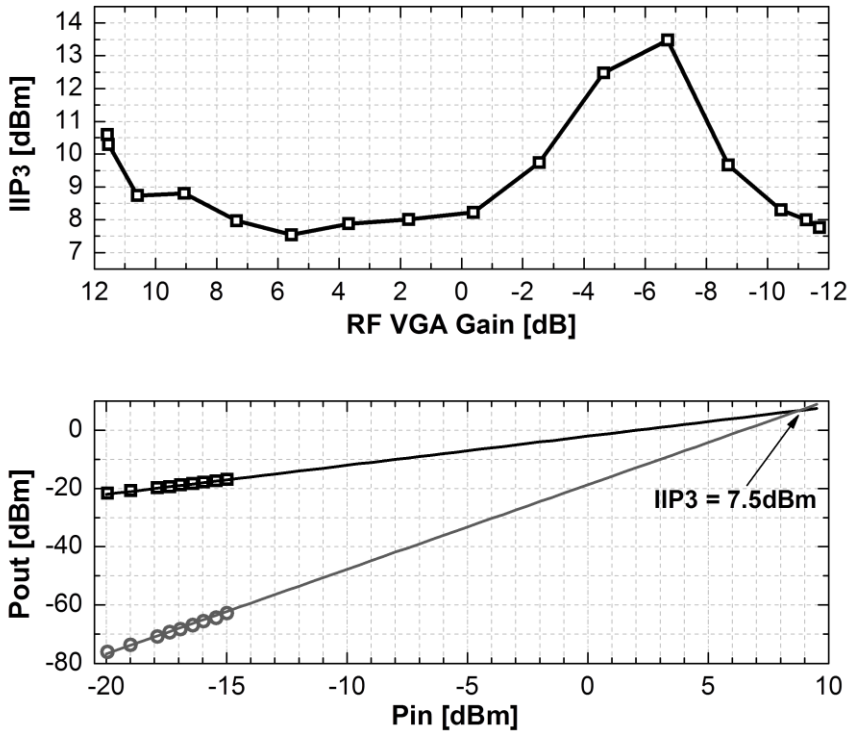


Figure 3.15 (a) Measured IIP_3 at different control voltage and (b) measured IMD_3 at the critical control voltage

selected to be 3 MHz (slightly smaller than the signal bandwidth, 3.84 MHz, of the WCDMA standard) and centered at 1950MHz (WCDMA band I). The worst-case IIP_3 is 7.5 dBm over all the gain settings at 1950 MHz. A trade-off for the linearity is the power consumption. This RFVGA consumes 11 mA from a 1.8-V power supply at DC, but the value increases to 12 mA with -5 dBm input power and to 15 mA with 0 dBm input power.

The shape of the IIP_3 curve of this RF VGA resembles that of a π-type attenuator alone [38]. This can be explained with the equation for the IIP_3 of cascade stages [3]:

$$IIP_{3,O}^2 = \left(\frac{1}{IIP_{3,1}^2} + \frac{A_{V1}^2}{IIP_{3,2}^2} \right)^{-1} = \left(\frac{IIP_{3,1}^2 \times IIP_{3,2}^2}{Av_1^2 \times IIP_{3,1}^2 + IIP_{3,2}^2} \right) \quad (3.4),$$

where $IIP_{3,O}$, $IIP_{3,1}$,and $IIP_{3,2}$ are IIP_3 of the whole RF VGA, the amplifying stage and the tuning stage in volts, respectively. In addition, A_{V1} is the voltage gain of the amplifying stage. The amplifying stage provides a large gain in this RF VGA circuits, making $A_{V1} \times IIP_{3,1}^2$ a dominant of the denominator of (3.4). Therefore, the overall IIP_3 of the RF VGA can be approximated as:

$$IIP_{3,O}^2 \approx \left(\frac{IIP_{3,1}^2 \times IIP_{3,2}^2}{Av_1^2 \times IIP_{3,1}^2} \right) = \frac{IIP_{3,2}^2}{Av_1^2} \quad (3.5),$$

which is determined by the IIP_3 of the tuning stage. Although P_{1dB} has a similar cascade equation, it assumes that different stages in the cascade have similar gain compression characteristics, which is not the case in this RF VGA. The gain compression of the amplifier is cancelled out by the reducing attenuation of the tuning stage at a higher input power, thus giving the RF VGA a different shape of P_{1dB} curve as compared to that of IIP_3.

Figure 3.16 illustrates the noise figure (NF) of the amplifier under different gain settings. The minimum NF of this work is 4.9 dB at 1.95 GHz, while it is 6.5 dB at 850 MHz. Figure 3.17 plots the values at different gain settings. The input amplifier of this RF VGA minimizes the noise contribution from the attenuator, thus giving the RF VGA a comparable NF at its lower gain settings as comparing to previously reported RF VGAs [23], [40]-[42]. As a further improvement, the input resistive matching (R_{IN} in Figure 3.10) can be replaced with inductive/capacitive matching networks to reduce the noise generated by the matching resistor, but this would incur the cost of larger die area. The specification of the proposed attenuator is summarized and compared in Table 3.1.

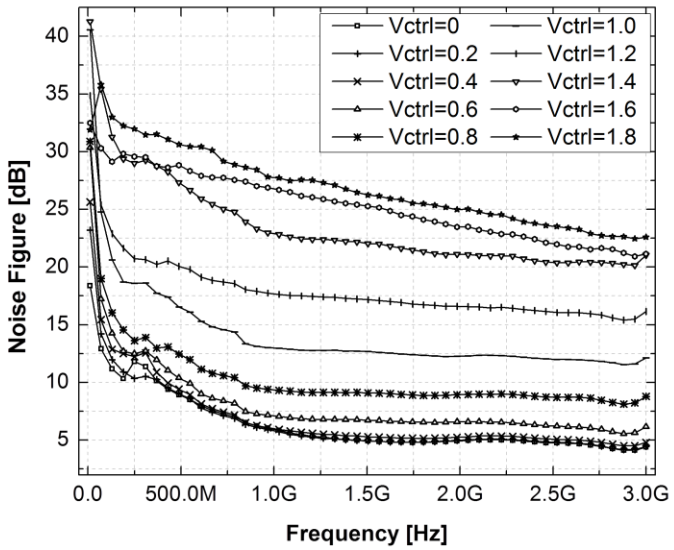


Figure 3.16 Measured noise figure of the RF VGA over different frequencies and at different gain settings

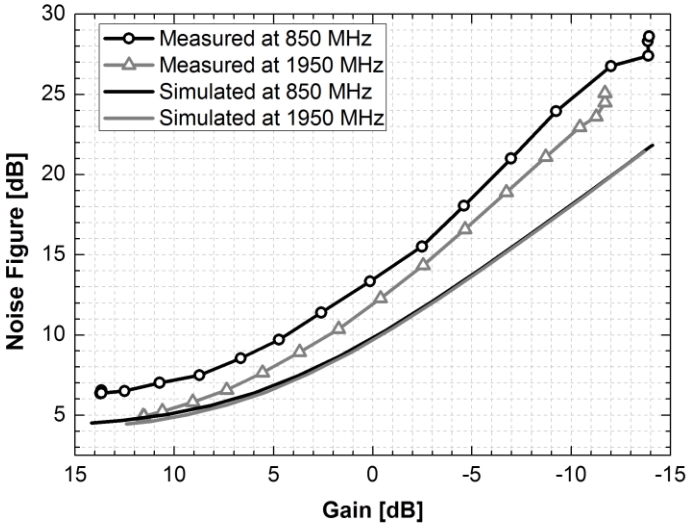


Figure 3.17 Measured noise figure of the RF VGA over different frequencies and at different gain settings

Table 3.1 Summery of Experimental Results for the VGA

References		Process [CMOS]	Frequency [GHz]	Area [mm^2]	Gain [dB]	min. P_{1dB} [dBm]	min. IIP_3 [dBm]	NF when gain is		Power [mW]	Control
								-5dB	-11dB		
JSSC 07[23]		0.18-μm	0.47 ~ 0.87	0.32	16 ~ -17	NA	-1.5	22dB	30dB	22	Digital
ASSCC 08[40]		0.18-μm	0.05 ~ 0.86	0.29	15 ~ -16	NA	2.6	22dB	30dB	10	Digital
TMTT 09[41]		0.18-μm	0.048 ~ 1	0.25	16 ~ -34	-15	-1	13dB	20.5dB	30.6	Digital
RFIC 09[42]		0.18-μm	0.03 ~ 1.4	0.0336	15.5 ~ -6.5	NA	3.7	23.5dB	NA	6.48	Digital
RFIC 08 [43]		0.18-μm	~ 2	NA	50 dB range	6 (OIP_3)	NA	NA	NA	56.3	Digital
EL 07[44]		0.18-μm	2.2/5.2	NA	5.1 ~ -8.9	-10	3	9dB	NA	NA	Analog
ISSCC 04[45]		0.18-μm	2±5%	0.7	34 ~ -16	NA	NA	NA	NA	40**	Analog
RFIT 07[46]		0.18-μm	0.43 ~ 2.33	0.41	9.5 ~ -3.3	-9	NA	NA	NA	16.2	Analog
RWS 10 [47]		0.13-μm	1.7 ~ 2	NA	25 dB range	NA	NA	NA	NA	54	Analog
This work	**0.85 GHz**	**0.18-μm**	**0.38 ~ 2.2**	**0.108**	**13.5 ~ -13.5**	**-5**	**5.7**	**18.5 dB**	**25.5 dB**	**19.8**	**Analog**
	1.95 GHz				**11.5~-11.5**	**-3.6**	**7.5**	**17 dB**	**23.5 dB**		

*do not exactly mention the worst-case ** including measurement buffer

CHAPTER 4

AN ULTRA COMPACT VARIABLE PHASE SHIFTER FOR ANALOG PREDISTORTION SYSTEMS

4.1 INTRODUCTION

A phase control circuit is another critical block for reducing the distortion of a PA. As stated in chapter 1, however, conventional variable phase shifters are either bulky or power hungry, and are not suitable for the Predistortion role. To find a suitable topology and make reasonable tradeoffs, we should first analyze the required features for such phase predistorter.

The phase shifter is used mainly to compensate for the phase variation at different power level. Since the phase error of most of the PAs are smaller than 20°[1], [48]-[50], this phase predistorter does not need a full 360° of phase control range, but a very accurate phase control curve to minimize the phase error within a relatively small range. Therefore, a continuously controlled phase shifter is greatly preferred over a discrete one, since the later needs a very huge binary array and an ADC to reduce the tuning step. In addition, a small size is also an important requirement for this shifter. A bulky phase shifter will increase the overall die area of the PA system dramatically, and so does its cost. Without the advantage of low production cost, a bulky CMOS PA system cannot compete against a III-V compound PA at all. Moreover, such a phase predistorter requires a small gain variation over the whole phase control range, since it is excluded from an amplitude predistortion loop to avoid unstable conditions.

All these requirements restrict the designer from directly applying the conventional VPS

topology to the pre-distortion system. The requirement on size restricts the use of a synthetic-transmission line or a passive RTPS. As aforementioned in chapter 1, the size of these types of phase shifters could sometimes be as large as that of a reported PA design, making them unsuitable for the predistortion application. Using an active circulator or active inductors can effectively reduce the size of a phase shifter, but the trade-off is their relatively high power consumption and sometimes a large gain variation over the tuning range. These drawbacks degrade the power efficiency, and increase the AM-AM error of the system, respectively. Accordingly, traditional phase shifters are not suitable for such an application. They either have a very large size and a phase-shifting range far exceeds the requirement; or consumes too much power, having excessive gain variation over the tuning range.

In response to the special demand of the PA predistortion system, a very compact, power efficient, and continuously controlled phase shifter that is much suitable for such application is presented in this chpter. It is based on a vector-sum structure similar to [51], but utilizes a modified RC poly-phase filter (PPF) to both reduce the size and relax the bandwidth-loss tradeoff. Besides, the summing amplifier along with a proposed controlling block is able to achieve a quasi linear-in-degree phase tuning capability, having a small gain variation. The schematic diagram of the proposed VPS is shown in Figure 4.1, and the analysis of these key deign blocks and the performance variation caused by RC value deviation will be given in Section II. The measurement results and a comparison to previous VPS works will be demonstrated in Section III.

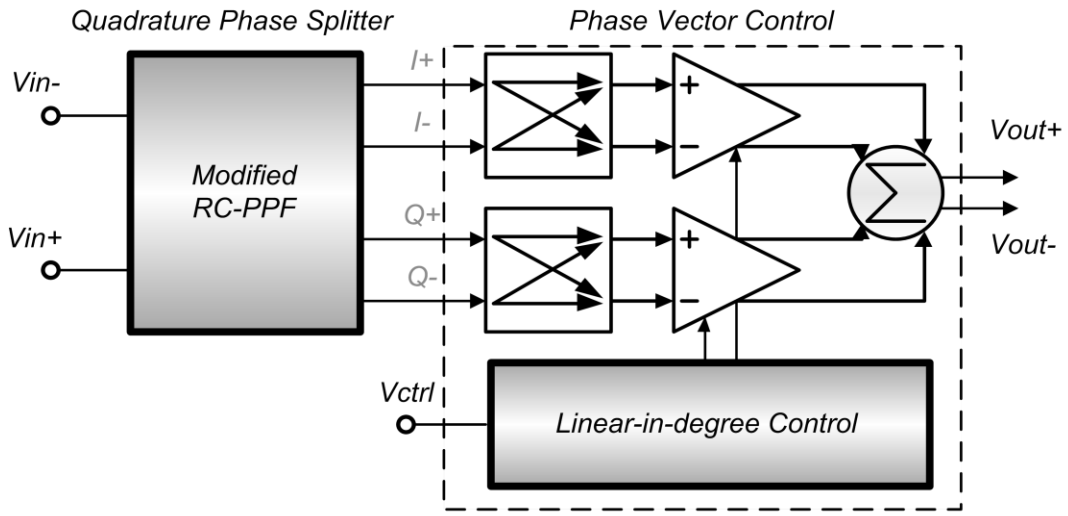


Figure 4.1 The circuit structure of the proposed variable phase shifter

4.2 DESIGN DETAILS AND ANALYSIS

Vector-sum phase shifters are known for its compact size, a better control of the phase and a smaller gain variation [51]. It utilizes a quadrature phase splitter to generate a set of orthogonal phase vector. By properly changing the magnitude of I and Q vectors, the phase of the VPS output signal could be tuned within a quadrant.

Using a hybrid coupler or LC all pass filter as the phase splitter are common manners in microwave circuits; but again, their bulky size limits how compact the VPS can be. Fortunately, for lower frequency applications like mobile communication and for just producing quadrature phase, it is possible to use a RC PPF as a much compact substitute. Its major disadvantages, higher loss and higher noise due to resistors, are not far beyond an acceptable range at lower giga-hertz frequency and for transmitters. Making a reasonable tradeoff or a modification to the traditional PPF design is able to resolve the problem.

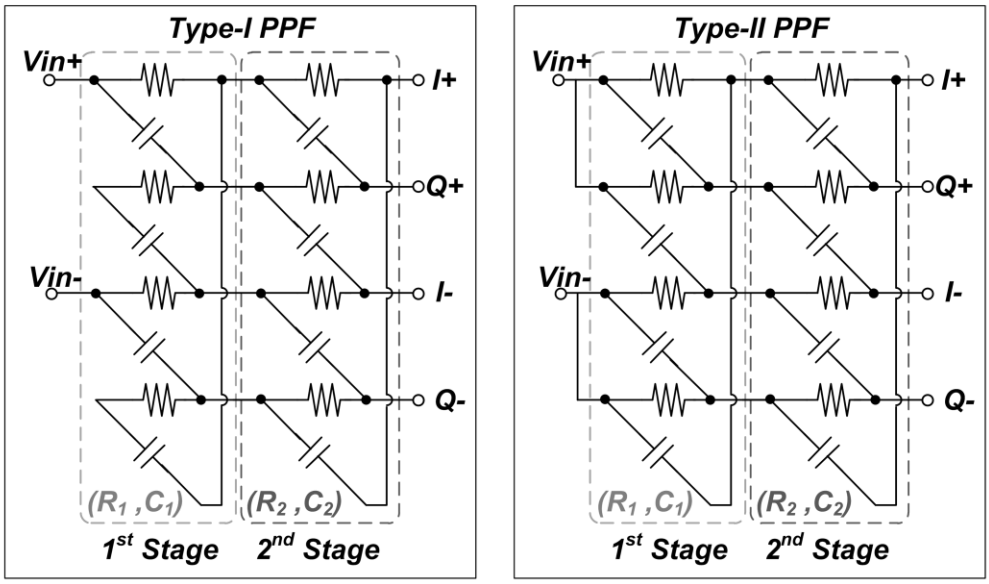
The controlling block is another circuit that needs to be redesigned. Most of the vector-sum

phase shifter uses digital mechanism to linearly control the phase, and to extend the phase tuning range to all four quadrants (360°). If the phase shifter is using an analog control, the tuning range will be limited to one quadrant. This is because, unlike digital switched control, analog control circuits can only turn off either I^+/I^- or Q^+/Q^- branches completely, but cannot switch I+ with I- or Q+ with Q- to extend the phase shifting range to the other quadrants. Moreover, a specially designed control block is required to get both a linear-in-degree phase control curve and a constant gain within the control range.

A modified PPF and a phase control circuit will be introduced and analyzed in this section. They together help reduce the size of the shifter, give the proposed design a linear-in-degree phase control curve, and minimize the gain variation.

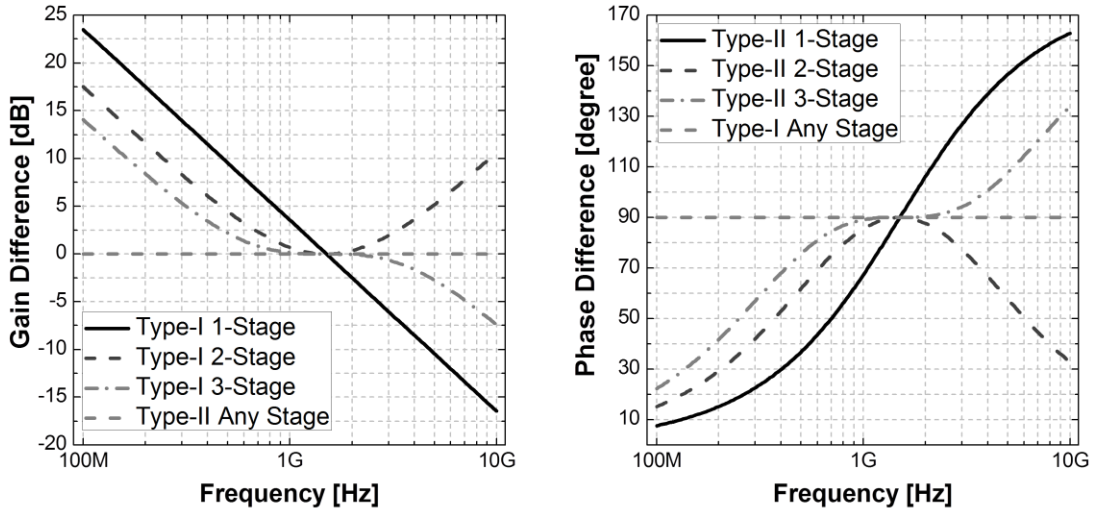
4.2.1 RC Poly Phase Filter

RC PPF has long been used in RF front-end designs for I/Q signal generation and image rejection [52]. According to the input configuration, RC PPF can be categorized into two types, as illustrated in Figure 4.2. For the same number of stages, the gain on the I and Q ports of type-I PPF matches within a narrower bandwidth, while a type-II PPF has a narrower I and Q phase-separation bandwidth where the phases of I and Q ports differ by exactly 90° [53]. To cover most of the mobile communication uplink, the phase predistorter is targeted to achieve at least 1 GHz of bandwidth. Consequently, multiple RC stages are necessary in the PPF design. According to the simulation results in Figure 4.3, no matter which types of PPF are using, we need at least three stages to get either a sufficient gain-match or a phase-separation bandwidth. However, the size, the wiring complexity, and the loss increase with the number of stages, necessitating a new topology that uses minimized stages to achieve a maximum bandwidth.



(a) (b)

Figure 4.2 (a) Type-I and (b) Type-II traditional RC poly-phase filters.



(a) (b)

Figure 4.3 The gain mismatches (a) and phase splitting (b) of traditional RC poly-phase filters with different number of stages.

This new topology is preferred to behave similar to a type-II PPF. A type-I PPF is much band-limited in its gain response, and so does the active summing amplifier. These leave the

VPS designed with the type-I PPF a smaller tolerated margin for gain variation (which is highly possible to occur considering the RC variations in real CMOS process). On the other hand, the phase mismatch from a type-II PPF only reduced the maximum phase control range, and contributes minor gain mismatch that can be compensated by a carefully designed control circuit.

We first investigate the transfer characteristics of a type-II PPF. The signal ratio between the *I* and *Q* ports of a two stage, type-II phase shifter can be written as [52]:

$$H(s)=\frac{I^{+}(s)}{Q^{+}(s)}=\frac{1-s(R_1C_1+R_2C_2)-s^2R_1C_1R_2C_2}{1+s(R_1C_1+R_2C_2)-s^2R_1C_1R_2C_2}, \tag{4.1}$$

where the phase of $H(s=j\omega)$ is 90° if ω equals to $1/R_1C_1$ or $1/R_2C_2$. It is able to get a similar transfer function with less RC components. For the modified PPF circuit shown in Figure 4.4, the transfer function of V_1 in terms of V_{in}^{+} and V_{in}^{-} is:

$$V_1(s)=\frac{1}{1+sR_aC_a}\left(V_{in}^{+}-V_{in}^{-}\right)+V_{in}^{-} \quad . \tag{4.2}$$

With an ideal differential input, V_{in}^{+} equals to $-V_{in}^{-}$, and we could rewrite (4.2) as:

$$V_1(s)=\frac{1-sR_aC_a}{1+sR_aC_a}V_{in}^{+} \quad . \tag{4.3}$$

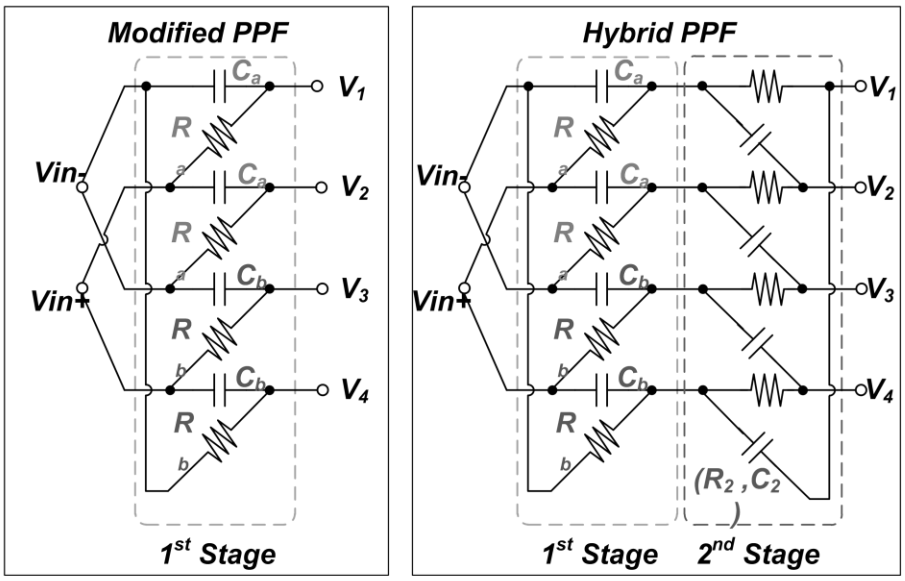
Similarly, $V_3(s)$ can be calculated as:

$$V_3(s)=\frac{1-sR_bC_b}{1+sR_bC_b}V^{+} \ . \tag{4.4}$$

The ratio between $V_1(s)$ and $V_3(s)$ turns to be:

$$H(s)=\frac{V_1(s)}{V_3(s)}=\frac{1-s(R_aC_a-R_bC_b)-s^2R_aC_bR_aC_b}{1+s(R_aC_a-R_bC_b)-s^2R_aC_aR_bC_b} \ , \tag{4.5}$$

which is similar to the transfer function (4.1) of a 2-stage type-II PPF. Assuming $R_aC_a > R_bC_b$ and solving (4.3) for $\angle H(s=j\omega) = 90°$, we can get:



(a) (b)

Figure 4.4 The circuit structure of the proposed variable phase shifter. (a) Type-M: 1-stage PPF that generates the same phase splitting as a Type-II PPF, and (b) Type-H: a hybrid of Type-M and a traditional PPF stage

$$1+\omega^2 R_a C_a R_b C_b = \omega\left(R_a C_a - R_b C_b\right) , \tag{4.6}$$

where ω in (4.6) has two real solutions if:

$$R_a C_a \geq (3+2\sqrt{2})R_b C_b . \tag{4.7}$$

For example, if $R_aC_a = 6R_bC_b$, the phase of $H(j\omega)$ will be 90° , when ω equals to $1/(2R_bC_b)$ *or* $1/(3R_bC_b)$. This not only proves that the modified 1-stage RC PPF is able to generate a set of orthogonal phase vectors, but the resulting relation between ω and RC value also allows the designer to use a smaller capacitor for the PPF design. The size of the modified PPF is therefore smaller than a type-I or -II PPF.

However, the V_1 and V_3 ports of the modified PPF are not symmetrical in terms of the RC value connected, and may produces gain mismatch. Although mismatch is very small if V_1 and V_3 are connected to a very high impedance load, the capacitive input impedance of the later stage vector-sum amplifier will cause a gain mismatch between these two ports. This mismatch should be minimized to reduce the design difficulties for the later-stage amplifier to have a linear phase control curve and a small gain variation. Therefore, as shown in Figure 4.4(b), a traditional RC stage is inserted between the modified PPF and the amplifier, giving an extra flexibility when making a tradeoff between a gain mismatch and I/Q split.

Figures 4.5 and 4.6 show the simulation results of type-II PPFs, a modified PPF (type-M), and a hybrid PPF (type-H). The type-M and type-H PPFs are the circuits demonstrated in Figures 4.4(a) and 4.4(b), respectively. All the designs are optimized for the smallest loss and then widest I/Q split bandwidth. A 1-stage type-M PPF has a similar I/Q splitting bandwidth as compared to a 2-stage type-II PPF, but with smaller losses. However, the gain mismatch between

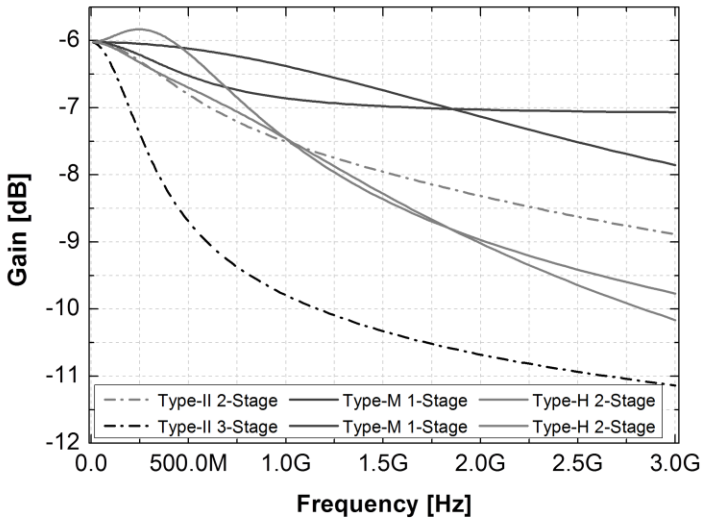


Figure 4.5 Gain versus of different types of PPF. For type-II PPF, the gain on all the ports are the same, while type-M and type-H PPF has gain mismatch between their I/Q ports.

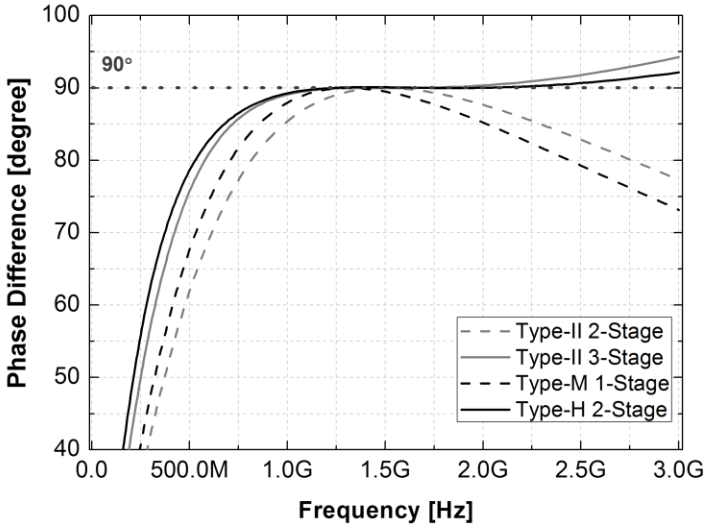


Figure 4.6 The phase splitting between I and Q ports of different types of PPF

the ports of a type-M PPF could be as much as 0.3 dB within the I/Q splitting bandwidth, while they are well matched all over the simulated frequency for a type-II PPF. A type-H PPF resolves the mismatch problem and shows only 0.08dB gain mismatch within the I/Q splitting bandwidth. In addition, the proposed type-H PPF successfully generates an I/Q splitting over a bandwidth even wider than that of a 3-stage type-II PPF and with 2-dB less loss, demonstrating its ability in a vector-sum type phase shifter.

4.2.2 Vector-Sum Amplifier

The magnitude of the I and Q signals generated by the PPF is adjusted and combined to be a new phase vector by the vector-sum amplifier. As shown in Figure 4.7, the amplifier has separated current sources for its I and Q differential pairs. The small signal output voltage of the amplifier can be written as:

$$Vout = g_{m,I} R_L V_I + g_{m,Q} R_L V_Q \ . \tag{4.8}$$

where V_{out} is the differential voltage at the output, V_I and V_Q are the differential input for I/Q signal, respectively. In addition, $g_{m,I}$ is the transistor transconductance for M_{N1} and M_{N3}, while $g_{m,Q}$ is the transconductance for M_{N2} and M_{N4}. Assuming the PPF generates a perfectly matched I and Q, V_I and V_Q can be written as $Vcos(\omega t)$ and $Vsin(\omega t)$, respectively, while V_{out} becomes:

$$Vout = g_{m,I} R_L V \cos(\omega t) + g_{m,Q} R_L V \sin(\omega t)$$

$$= R_L V \times \sqrt{g_{m,I}{}^2 + g_{m,Q}{}^2} \times \left[\frac{g_{m,I}}{\sqrt{g_{m,I}{}^2 + g_{m,Q}{}^2}} \cos(\omega t) + \frac{g_{m,Q}}{\sqrt{g_{m,I}{}^2 + g_{m,Q}{}^2}} \sin(\omega t) \right]$$

$$= Av \sin(\omega t + \varphi) \qquad (4.9),$$

where

$$\begin{cases} \mathrm{Av} = R_L V \times \sqrt{g_{m,I}{}^2 + g_{m,Q}{}^2} \\ \varphi = \sin^{-1}\left(g_{m,I} \Big/ \sqrt{g_{m,I}{}^2 + g_{m,Q}{}^2} \right) \end{cases} . \qquad (4.10)$$

To get a constant gain (Av) at all phases, it is required that

$$g_{m,I}{}^2 + g_{m,Q}{}^2 = \frac{1}{2}\left(I_I + I_Q \right) = Constant \ , \qquad (4.11)$$

where N is the sizing scalar between M_{NSI}, M_{NSQ} and M_{NS1}, M_{NS2} Therefore, if the bias currents of I and Q branch are controlled properly, this phase shifter could have a constant gain. To generate these two bias currents, the proposed phase shifter uses a bias control circuit, as shown in Figure 4.8. Considering the case when $R_P = R_N = 0$ and for a small V_{CTRL} variation near the bias point, the current on M_{NS1} and M_{NS2} can be written as [36]:

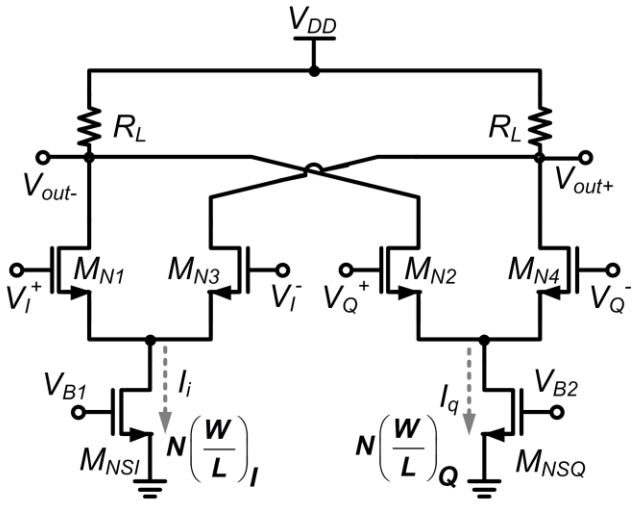


Figure 4.7 The schematic diagram of the vector-sum amplifier

$$\begin{cases} \Delta \mathrm{I}_1 = m \times g_{mN} \times \Delta V_{CTRL} \\ \Delta \mathrm{I}_2 = g_{mP} \times (-\Delta V_{CTRL}) \end{cases} \tag{4.12}$$

If $m \times g_{mN} = g_{mP}$, $\Delta I_1 + \Delta I_2$ equals to zero and hence $I_1 + I_2$ is a constant regardless of V_{CTRL}. If I_1 and I_2 are mirrored directly to I_I and I_Q, the vector-sum amplifier will then have a constant gain (Av).

The other feature this control circuits need to provide is a linear-in-degree control curve. As shown in (4.10), the phase (φ) is related to g_m through an inverse sine function. The Taylor expansion of an inverse sine can be written as:

$$\begin{cases} \varphi = \sin^{-1}(x) = x + \frac{1}{2}\frac{x^3}{3} + \frac{1}{2}\frac{3}{4}\frac{x^5}{5} + \frac{1}{2}\frac{3}{4}\frac{5}{6}\frac{x^7}{7} + \cdots \quad |x| < 1 \\ x = g_{m,I} \Big/ \sqrt{{g_{m,I}}^2 + {g_{m,Q}}^2} \end{cases} \tag{4.13}$$

For a small x, φ can be approximated by x:

$$\varphi \approx x = g_{m,I} \Big/ \sqrt{{g_{m,I}}^2 + {g_{m,Q}}^2} \propto K_N^{'}(V_{CTRL} - V_{TN}) \tag{4.14}$$

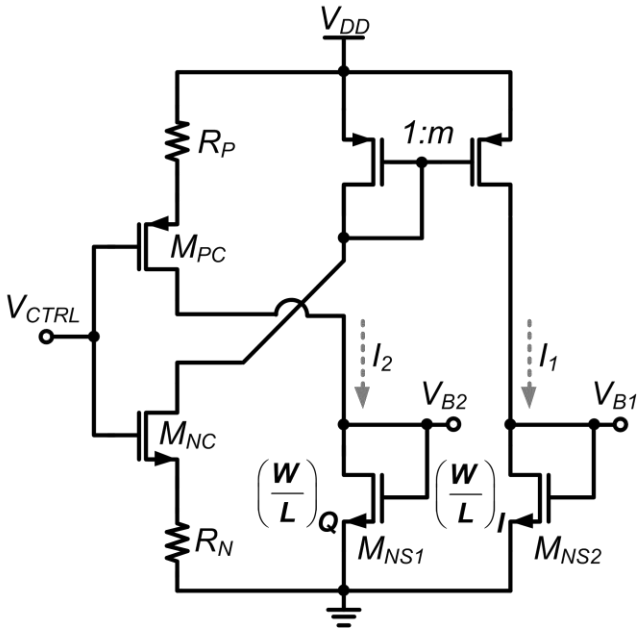


Figure 4.8 The schematic diagram of the control circuit for the vector-sum amplifier

where K_N is a process and size related parameter of M_{NC}. A linear relation between the variation of φ and the variation of V_{CTRL} is clearly shown in (4.14). Figure 4.9 illustrates the simulation results for gain, phase, and current of the vector-sum amplifier controlled by the proposed structure without R_P and R_N. Because of the square-law behavior of the transistor, the bias current only maintains relatively constant in a very small range; and the phase versus control is not nicely a linear curve as predicted. The gain, on the other hand, stays constant for all the control range. It is because the exceeding bias current drives the I or Q branches into triode region when V_{CTRL} is either very high or low. The drops of g_m of transistors operating in their triode region compensate for the gain increase from a higher bias current, limiting the overall gain variation.

To get a better control of the phase, two degeneration resistors R_N and R_P are incorporated in

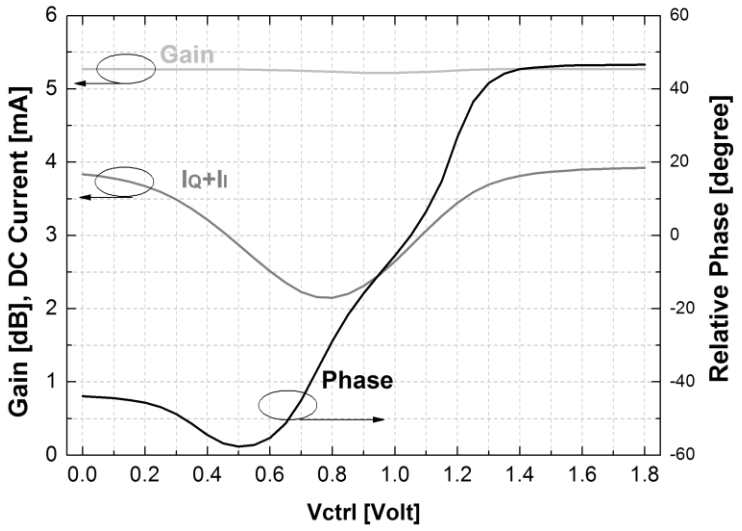


Figure 4.9 The gain, DC current and relative phase shifts of the vector-sum amplifier over the voltage controlled by the circuit shown in Figure 9 without R_N and R_P

the control circuit. These resistors linearize the current source (M_{NC} and M_{PC}), giving a constant bias current over a wider range. By optimizing the overall control circuits, the final design is able to get a much linear phase curve, as shown in Figure 4.10.

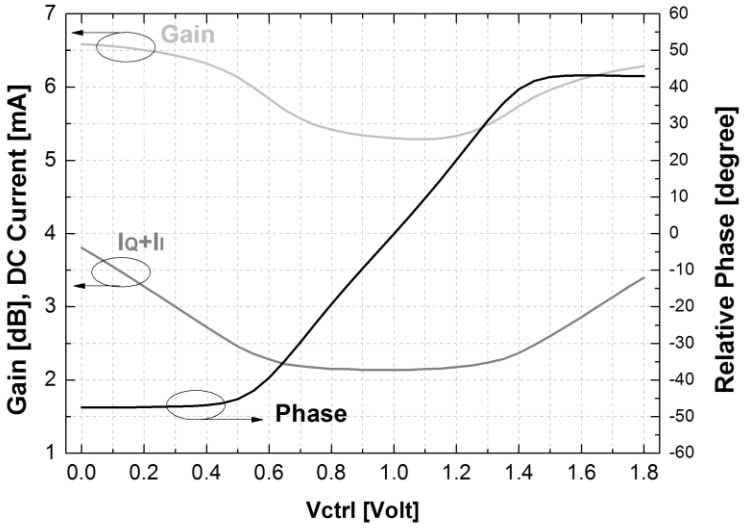


Figure 4.10 The gain, DC current, and relative phase shifts of the vector-sum amplifier over the voltage controlled by the circuit shown in Figure 9

This phase shifter uses many resistors and capacitors especially in the PPF stage. Since the RC values easily change from die to die, Monte Carlo simulations are performed to examine how the process variation on PPF affects the overall performance. Figures 4.11 and 4.12 show the

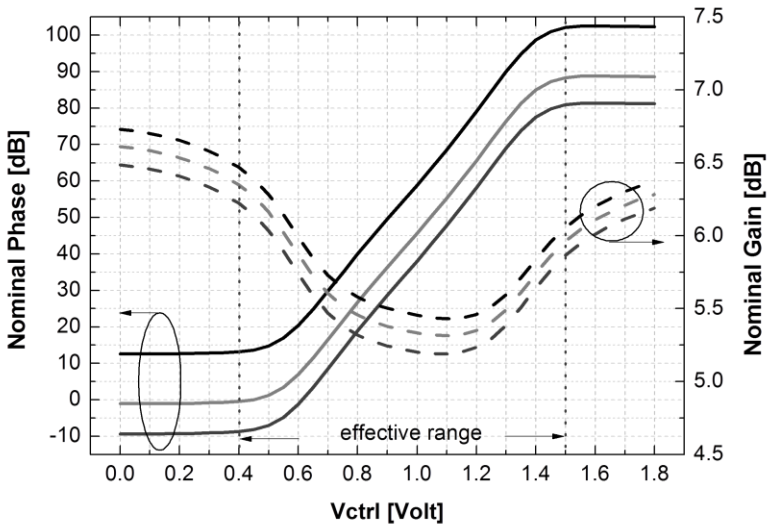


Figure 4.11 Phase/gain versus control voltage, the typical and extreme cases from Monte-Carlo simulations

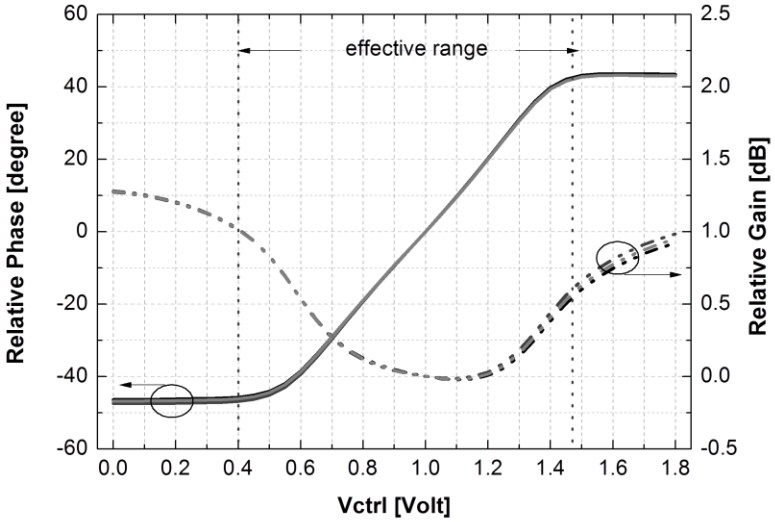


Figure 4.12 Relative phase/gain versus control voltage (refer to V_{CTRL}=1), the typical and extreme cases from Monte-Carlo simulations

typical and worst-case results assuming 20% variation for R and 10% for C. Although the nominal gain and phase values do vary, as shown in Figure 4.11, the relative value shown in Figure 4.12 for every dies is almost the same, meaning that each VPS could still correct the phase error without bringing too much gain variation.

4.3 MEASUREMENT RESULTS

Such a VPS optimized for WCDMA applications has been fabricated using the IBM CMRF7SF 0.18-μm CMOS process, and the die microphotograph is shown in Figure 4.13. The

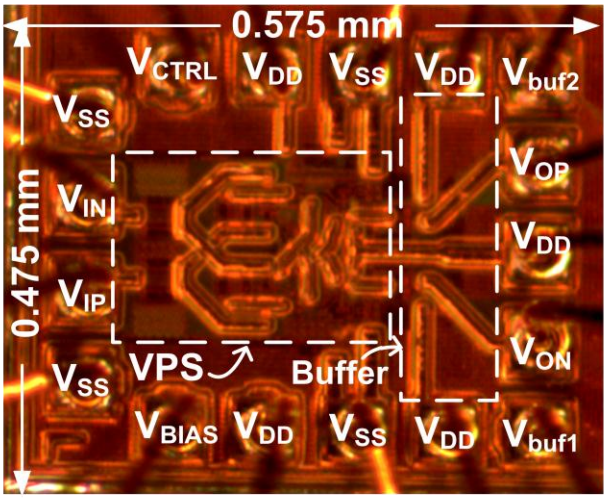


Figure 4.13 The die photograph of the variable phase shifter

active area of the VPS is 0.225×0.3 mm^2, while it is 0.475×0.575 mm^2 if the measurement buffers and pads are included. This die was mounted on a printed circuit board for a chip-on-board measurement.

The phase and gain of this circuit were measured with a 4-port network analyzer. Figure 4.14 plots the phase versus frequency at different gain settings. The VPS is able to achieve a

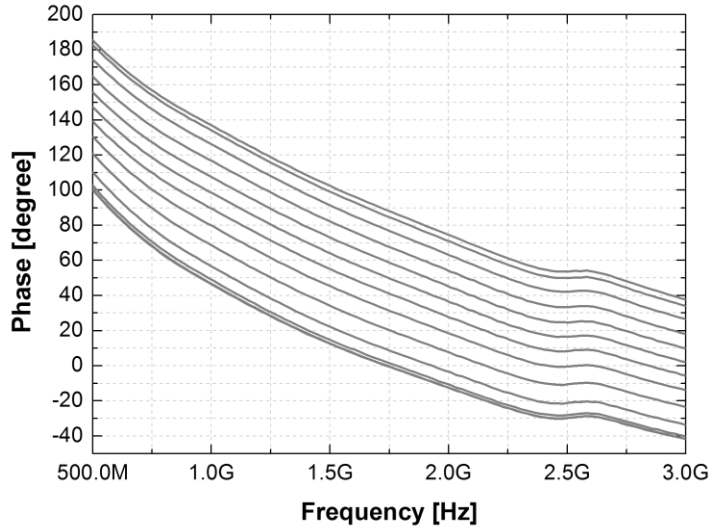


Figure 4.14 Measured insertion phase of the proposed variable phase shifter at different frequencies and phase setups

phase control range of 90° from 1 GHz to more than 3 GHz. The measured phase control curve at 1.95 GHz (WCDMA band I) is shown in Figure 4.15. The curve approximates a linear-in-degree relation when V_{CTRL} is within 0.5 V to 1.4 V range. The curve was fitted with a straight

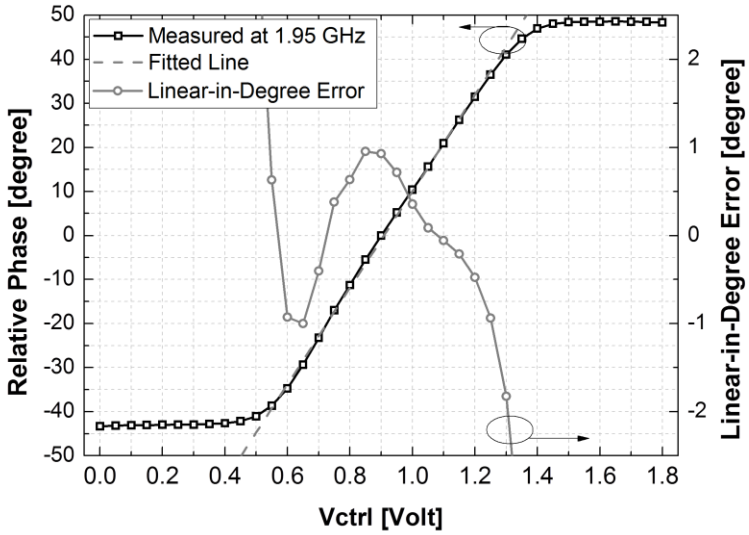


Figure 4.15 Measured phase control curve and linear-control error of the proposed variable phase shifter

line, and this fitted line to the actual control curve The VPS shows a phase control error less than ±1° within a phase variation range of 70°.

The gain of this VPS at different frequencies and settings are demonstrated in Figure 4.16.

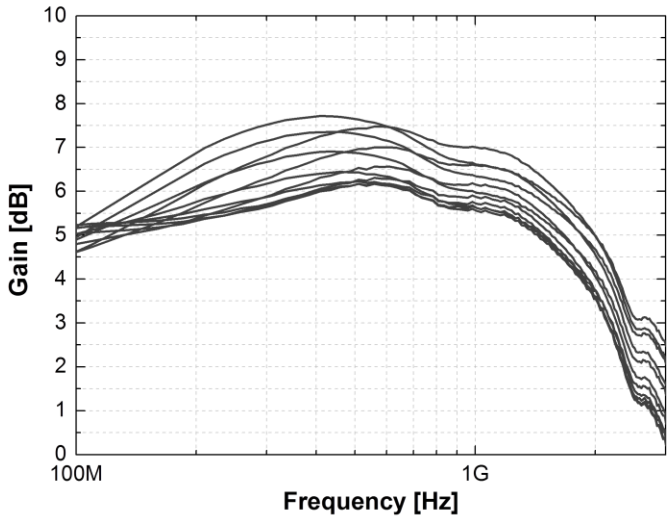


Figure 4.16 Measured gain response of the proposed variable phase shifter at different frequencies and phase setups

The 3-dB bandwidth of the VPS is from 80 MHz to 2.1 GHz. The functional bandwidth of the VPS is therefore from 1 GHz to 2.1 GHz, which is the intersection of the gain and phase bandwidth. Its gain variations over a whole 90° phase control range are around 1 dB at any frequencies.

Figure 4.17 plots the measured gain and linearity at different phase control settings. The output power at the 1-dB compression point (OP_{1dB}) is measured with a single tone at 1.95 GHz, while the output 3rd order interception point (OIP_3) is measured with a two-tone signal centered at 1.95 GHz and separated by 3 MHz. The tone spacing is smaller than the bandwidth of WCDMA signals (3.84 MHz). Measurement buffers are assumed much linear than the circuits, and therefore their nonlinear effects are not de-embedded. The worst-case OP_{1dB} and OIP_3 of the

VPS are -2 dBm and 10 dBm, respectively. The worst-case scenario happens when the V_{CTRL} are set in the middle of the phase control range. This is because the transistors in the differential pair of the vector-sum amplifier shown in Figure 4.7 are most closed to the triode region. When

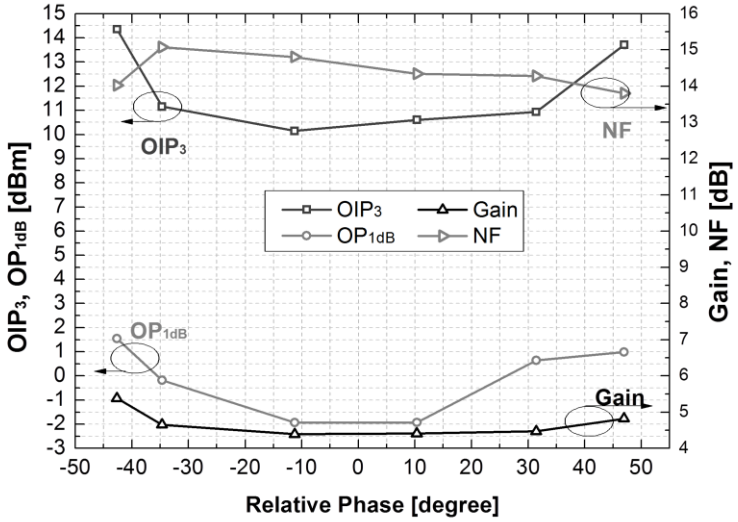


Figure 4.17 Measured OIP_3, OP_{1dB}, Gain and NF of the proposed variable phase shifter

V_{CTRL} is very high or very low, all the bias current passes through either I or Q branches, and the other branch is almost off. On the other hand, when V_{CTRL} is at the middle of the control range, the I and Q branches carry half of the maximum current. Since the input voltage bias is set to be the same value at all V_{CTRL}, the gate-to-source voltages at different V_{CTRL} are very similar. Therefore, the transistor has to go closer to the triode region when the bias current is small, resulting in an inferior linearity performance. The measured noise figure (NF) is shown in the same graph. The buffer was not de-embeded because it was found in the simulation that the gain of this VPS was high enough to suppress the NF contribution from the buffer. The maximum NF was 15.1 dB at 1.95 GHz and 12.8 dB at 1 GHz, respectively. The VPS draws a DC current of 2.3 mA from a 1.8-V power supply; the value remains a constant within the effective phase

control range. These parameters are summarized and compared with other CMOS works in Table 4.1.

Table 4.1 Summery of Experimental Results for the VPS

References	Freq. Range (GHz)	Phase Range	Area (mm^2)	Min. Gain (dB)	Gain Variation (dB)	Power (mW)	Max.NF (dB)	Topology	Process
ISSCC 04 [59]	2.27-2.45	105°	1.08	-16.9	9.2	0	16.9	RTPS	0.18-µm CMOS
ISSCC 04 [59]	2.27-2.45	105°	1.08	-11	6.4	1.8	16.9	RTPS	0.18-µm CMOS
TMTT 08 [58]	2.33-2.60	120°	0.72	-6.8	2.4	0	NA	RTPS	0.18-µm CMOS
TMTT 08 [58]	2.44-2.55	340°	0.66	-12.6	4	0	NA	RTPS	0.18-µm CMOS
TCAS-I [24]	1.71-2.07	>180°	0.7	-10	8	0	16.7	RTPS	0.18-µm CMOS
TCAS-I [24]	1.85-2.05	>360°	2.5	-7.3	8.2	2.16	14.5	RTPS	0.18-µm CMOS
TMTT 08 [25]	2.1-2.5	120°	0.357	-5	5	111	23.8	Active RTPS	0.18-µm CMOS
TMTT 07 [60]	1.5-3.5	96°	0.365	2.8	1	31.5	12.8	Synthetic TL	0.13-µm CMOS
TMTT 06 [54]	2.4/3.5/5.8	180°	2.76	-6.6	6.6	45	NA	DT	0.18-µm CMOS
RFIC 04 [55]	2.4/5.5	360°	NA	4	NA	28.8	NA	FTPS	0.18-µm CMOS
TMTT 10 [56]	2.5-3.2	360°	4.16	-2.5	3	60	18	Switched	0.18-µm CMOS
TCAS 10[57]	2.0-3.0	360°	0.38	1.5	3	24	15	Vector-Sum	0.18-µm CMOS
This work	**1.0-2.1**	**90°**	**0.06/0.27***	**4.8**	**1**	**4.2**	**14**	**Vector-Sum**	**0.18-µm CMOS**

*including IO pads

CHAPTER 5

SYSTEM SIMULATION OF AN ANALOG-PREDISTORTION PA SYSTEM IN CMOS TECHNOLOGY

5.1 SYSTEM OVERVIEW

To demonstrate the effectiveness of the proposed amplitude and phase predistorter, a complete predistortion-system simulation is performed in this chapter. In addition to the aforementioned amplitude-control and gain-control circuits, detection circuits are also included in the simulation. A more detailed block diagram of the system is shown in Figure 5.1.

The major parts of the system, including an amplitude error detector and a phase error detector, are implemented based on a commercial available 0.18-μm CMOS model. The amplitude error detector are composed of two logarithm amplifiers, as the power detectors for PA input and output, and a subtraction circuit designed with an OP-AMP. The phase error detector, on the other hand, are composed of two buffering amplifier and a Gilbert cell mixer. Besides, the core PA is implemented based on a known PA structure targeting for WCDMA application [65]. The VGA in Figure 5.1 is included in the phase error detection loop because the design introduced earlier has a high phase variation when sets at different gain settings. The VPS circuit in the simulated system is optimized for minimum gain variation and therefore can be placed outside the amplitude error detection loop.

This chapter is organized as follow. Section two gives a detailed design analysis of the amplitude/phase error detectors and their simulated performances. While in section three, an

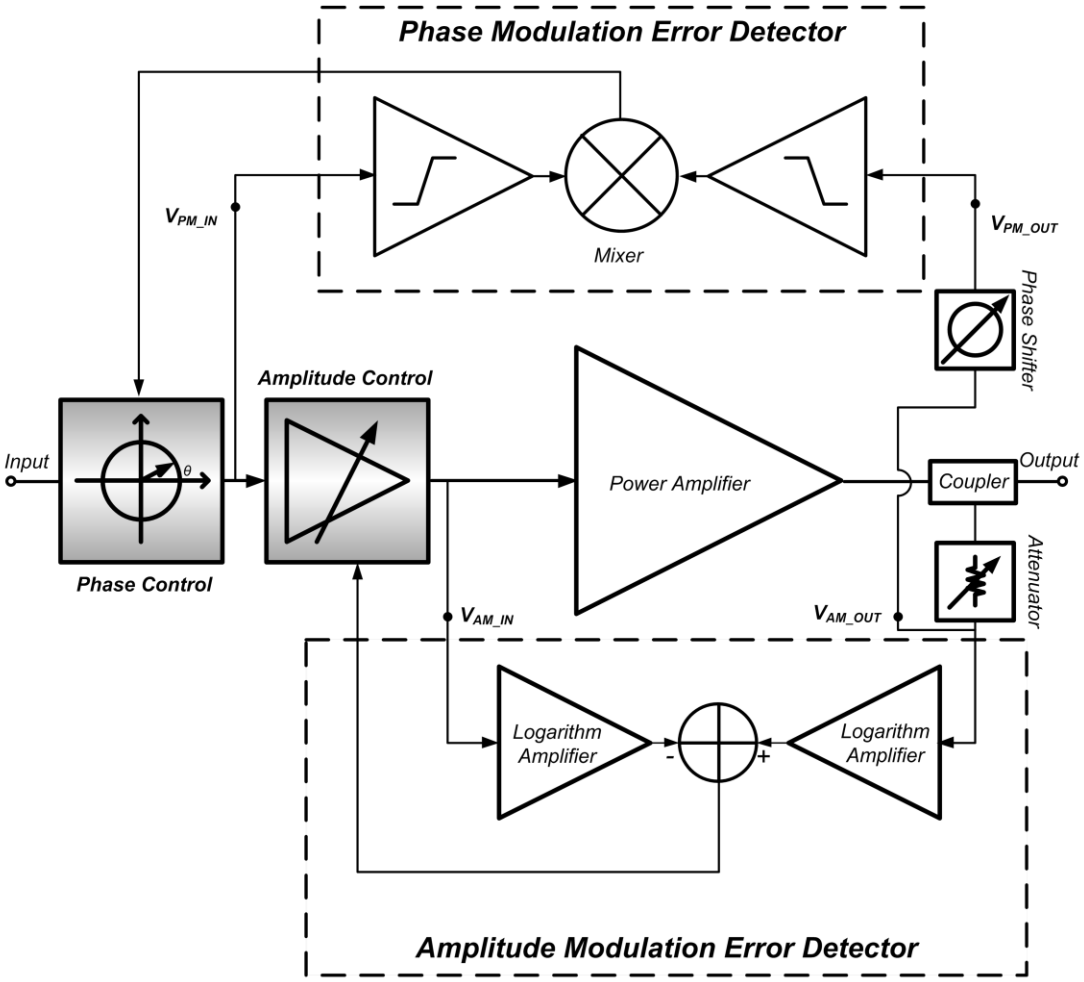


Figure 5.1 A more detailed block diagram for the circuits in the analog-predistortion PA system

analog predistortion system is built and optimized for WCDMA. Simulations such as a single-tone and WCDMA modulated signals will then be performed to evaluate the linearity performance. Gain/phase flatness, adjacent channel power ratio (ACPR), and EVM will be compared between PAs with and without predistortion.

5.2 AMPLITUDE AND PHASE DETECTION CIRCUITS

Circuits for amplitude detection are commonly used in receivers. They work with the VGA and form an automatic gain-control (AGC) loop to adjust the received signal strength for A/D converters [66]. Using logarithm amplifiers is the most popular way to implement the amplitude detection circuit because of its high dynamic range. The output of a logarithm amplifier is decibel-linear to its input signal strength, namely, for every dB-increment of the input power, output voltage increases by the same number of voltage. This exactly fits the requirement of an amplitude detection circuit in the analog predistortion system. If the relationship between the input power and the output voltage of a logarithm amplifier matches the control curve of the gain tuning VGA, the interfacing circuits between the detection and control block will be very easy to design. For example, if the output of the logarithm amplifier is X (Volt/dB) and the control curve of the VGA is X^{-1} (dB/Volt), the interfacing circuit will be just a level shifter that shifts the DC level to the center of the VGA control curve, reducing the complexity of the control circuits.

On the other hand, phase detectors are important components for any circuits require an accurate frequency synthesizer. A phase detector is a part of the phase-lock loop (PLL), and usually designed in digital domain. A circuit that has a continuous output-voltage versus input-phase curve is also commonly used in all receivers, but appears in the form of frequency mixer. Namely, a mixer can also be a phase detector if the signal to both RF and local oscillation (LO) ports are of the same frequency.

This section gives a brief introduction to the amplitude and phase detection circuits used in the simulation. The design considerations and simulation results based on the 0.18-μm CMOS model will be demonstrated.

5.2.1 A linear-in-dB Amplitude Detector designed with Logarithm Amplifiers

There are two ways to implement a logarithm amplifier: using bipolar junction transistors (BJT), or cascade-amplifier structure. The first solution exploits the exponential relation between the base-emitter voltage and the collector current of a BJT. However, a good BJT is hard to implement in a CMOS process and is not suitable for high frequency operation [67]. Therefore, the cascade-amplifier seems to be a more realistic solution for the mentioned CMOS predistortion system.

A cascade logarithm amplifier uses cascaded amplifiers with parallel current summing. The block diagram of such a logarithm amplifier is shown Figure 5.2. The input ports are connected to a series of amplifiers. When the input power increases, these amplifiers saturate consecutively.

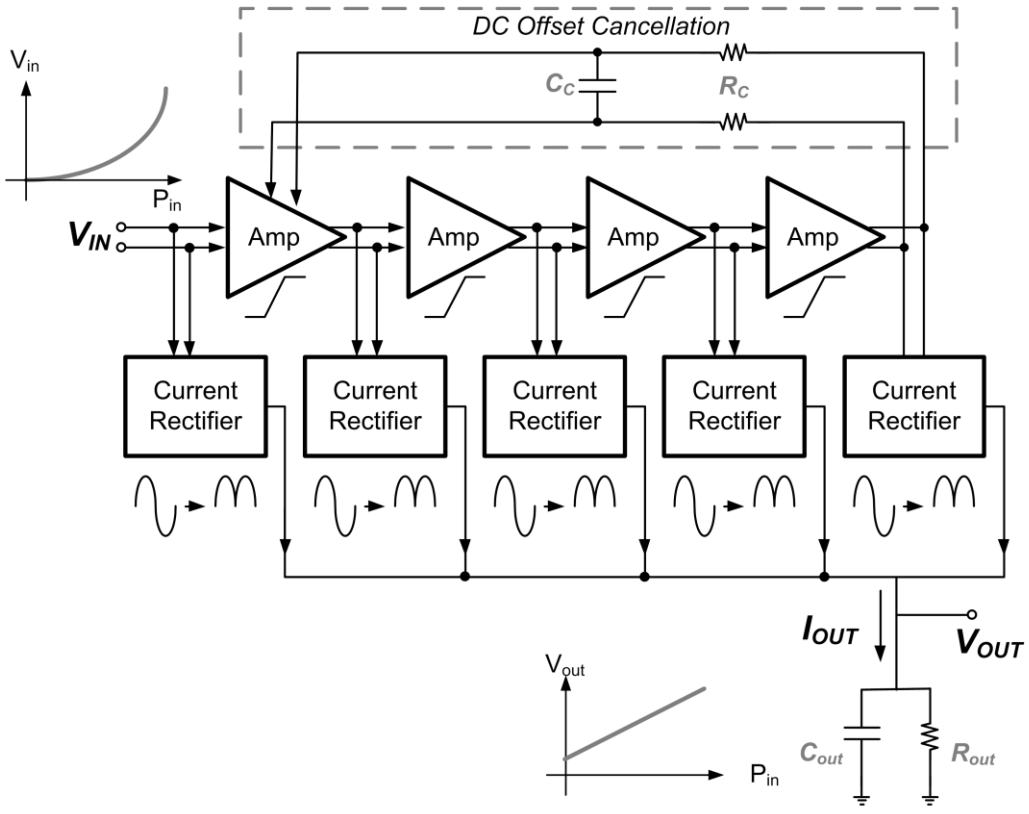


Figure 5.2 The block diagram of the logarithm amplifier

By summing the parallel current from each stage through a low-pass RC filter, a linear-in-dB input-versus-output relation can be achieved.

For example, if there are totally 4 stages of amplifier, each has a gain of 20-dB (nominal voltage gain equals to 10) and a saturated output voltage of 1-V peak-to-peak (V_{PP}). In addition, each rectifier has a g_m of 10mA/V_{PP}. Assuming a 50-Ω matched input, a -76 dBm input power (equals 0.1×10^{-3} V_{PP}) will saturate the output of the last (4th) stage of the cascaded amplifiers. Hence the output current measured from the last current rectifier will be 10 mA, while it is 1 mA (10 times smaller) from the 3rd stage, 0.1 mA from the 2nd stage, 10 μA for the 1st stage, and 1 uA from the input stage. The total current of the output is therefore 10 mA (4th stage) + 1.111 mA (from rest of the stages). Now if the input power is increased by 20 dBm, then it can be found that the 3rd and 4th amplifier stages are both saturated, generating a total 20 mA (3rd and 4th stage) + 1.11 mA (from rest of the stages) at the output. That is, for any 20-dB increment of the input power, the output current increases by around 10-mA (the slope is 0.5 mA/dB), demonstrating exactly a logarithm behavior. It is also noticed that a better dynamic range and a smaller logarithm error (the residual current from the non-saturated stages) come with a larger gain of each amplifier stage. An exact expression for log error can be written as [66]:

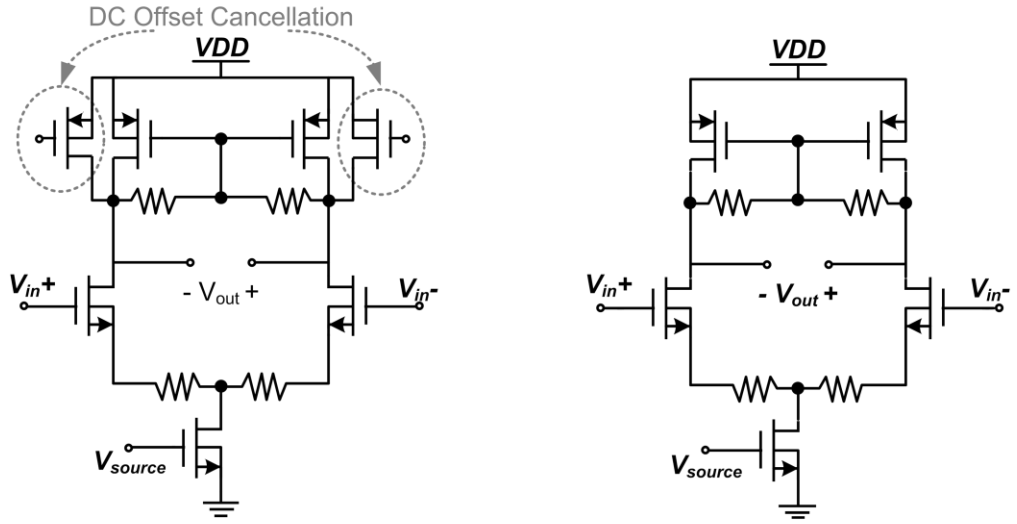
$$\mathrm{Error}_{\max}(\mathrm{dB}) = \frac{10\left[\left(-1+\sqrt{A_S}+A_S\right)\left(\log A_S\right)-\left(A_S-1\right)\log\left(A_S^{(3A_S-1)/(2A_S-2)}\right)\right]}{A_S-1} \qquad (5.1),$$

where A_S is the nominal voltage gain of each amplifier.

However, a large gain reduces the bandwidth of the logarithm amplifier. Fortunately, the dynamic range requirement for a power detector in the predistortion PA system is much relaxed than those in receivers. Therefore, the logarithm amplifier demonstrates in this section is maximized for high operation frequency while having reasonable errors. All the circuits on the

signal path, including the cascaded amplifiers and the current rectifiers are designed with minimum number of transistors to reduce the parasitic effects. The number of stages is also minimized to 4 amplifiers and to 5 current rectifiers.

Figure 5.3 shows the amplifier topology used in this design. Different from the traditional limiting amplifier, diode loads are replaced with simple resistive loads to reduce the parasitic. In addition, resistive degeneration resistors are used to limit the output swing and to improve the linearity. There are two different amplifier topologies shown in Figure 5.3, topology (a) is used as the first stage while the rest of the amplifier is using topology (b). To solve the DC offset



(a) (b)

Figure 5.3 The schematic diagrams of cascaded amplifiers: (a) the first stage that has DC offset cancellation, and (b) the remaining stages

problem faces by most of the logarithm amplifiers using cascade structure, the output of the last-stage amplifier will be connected to the loading transistor of the first-stage amplifier. This arrangement can greatly reduce the input referred DC offset voltage. The output of each

amplifier is then connected to a current rectifier, as shown in Figure 5.4. Two input transistors

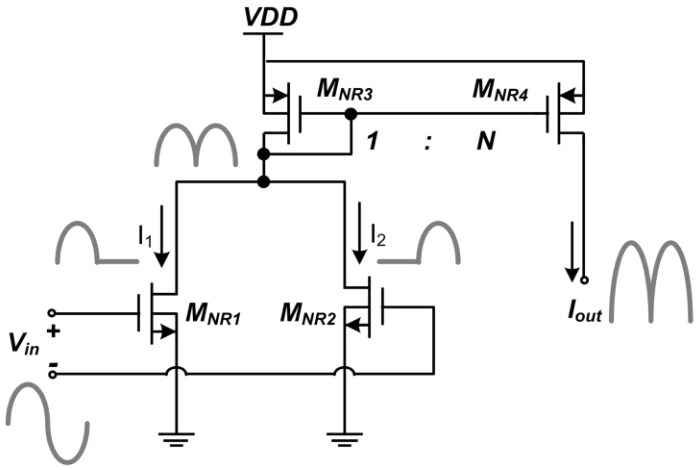


Figure 5.4 The schematic diagrams of the current rectifier

(M_{NR1} and M_{NR2}) are biased in class-B and produce output current when the voltage swings at their gate terminals are positive. Therefore, if the input is a sinusoidal wave, M_{NR1} and M_{NR2} conduct a current separately on different half-cycle. The current is then summed at M_{NR3} and mirror to M_{NR4} (I_{out}). Filtering out the AC components by a low pass filter, we can get a DC signal at the output of the current amplifier.

The simulation results of the logarithm amplifier are plotted in Figure 5.5. The dynamic range of this logarithm amplifier is from -30 dBm to 10 dBm. The logarithm-error of the output is less than ±0.2 dB from -27 dBm to 5 dBm. The input-versus-output curve has a slope of 0.03 Volt/dB. By changing the resistance value of the LPF, the slope could later be adjusted to fit the slope of the VGA control curve.

The amplitude modulation error detector (AMED) is composed of two logarithm amplifiers and an analog adder which implemented with an OP-AMP. The simplified schematic diagram of

the AMED is shown in Figure 5.6. An extra attenuator is put in the input of one of the logarithm

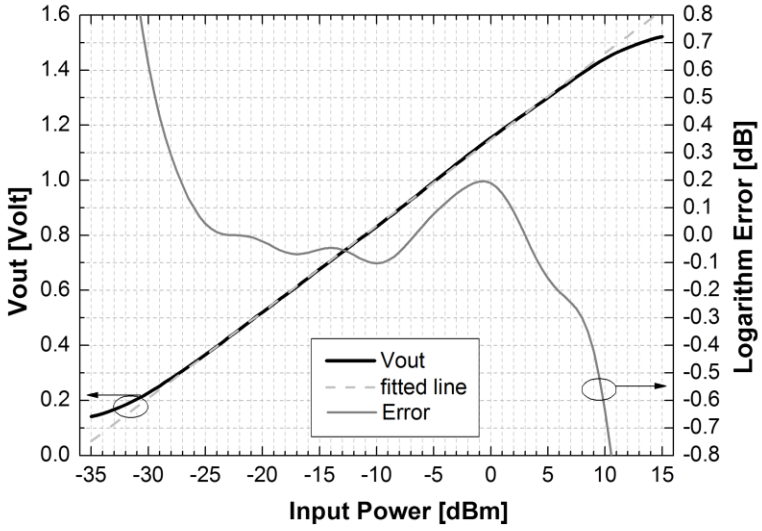


Figure 5.5 Input power vs. output voltage of the logarithm amplifier simulated at 1.95 GHz

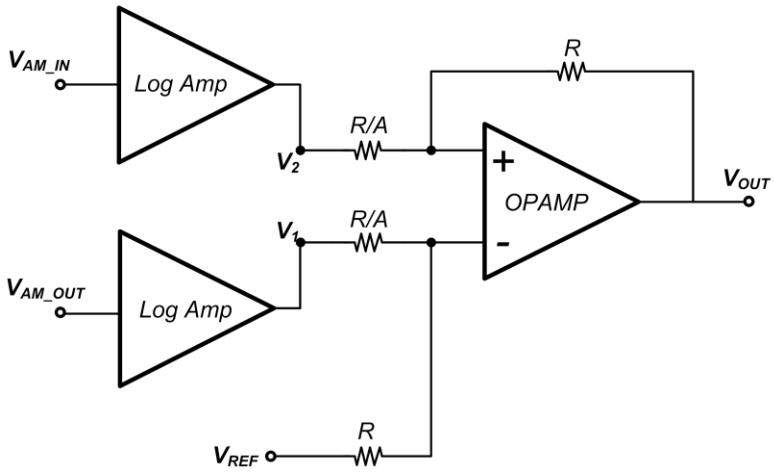


Figure 5.6 The schematic diagram of the AMED. It is implemented with two logarithm amplifiers and an analog adder.

amplifier to adjust the signal level, so that the amplitude of V_{AM_IN} in Figure 5.1 equals to V_{AM_OUT} when the input level is small and when the PA shows no gain-compression. The V_{OUT} of the AMED in Figure 5.6 therefore can be calculated as:

$$V_{OUT} = A(V_1 - V_2) + V_{REF} \quad (5.2).$$

By adjusting V_{REF} and the resistance values (R/A) those logarithm amplifiers connected to, we can easily matched the control curve of the amplitude controller to the output curve of the AMED.

5.2.2 A linear Phase Detector designed with Gilbert Cell

Phase modulation error detector (PMED) is another block required for building up the predistortion system. The work presented in this chapter uses a Gilbert cell mixer to perform the detection. Its schematic diagram is shown in Figure 5.7. Assuming the transistors in LO ports

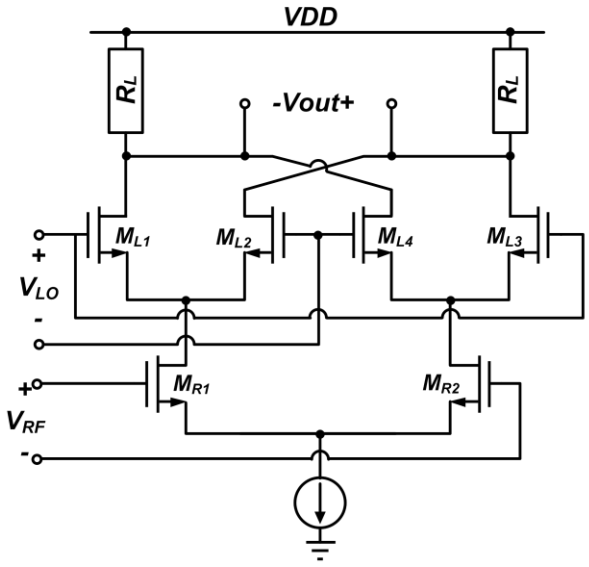


Figure 5.7 The schematic diagram of a Gilbert cell mixer

work as ideal switches, the differential output voltage of the mixer can be written as:

$$\text{Vout} = \frac{\pi}{2} g_m R_L \left[V_{RF} \cos\left(\omega_{RF} - \omega_{LO}\right) + V_{RF} \cos\left(\omega_{RF} + \omega_{LO}\right) \right] \quad (5.2),$$

where g_m is the transconductance of the RF transistors (M_{R1} and M_{R2}), V_{RF} the amplitude of input signal at RF ports, ω_{RF} and ω_{LO} the frequency of RF and LO signals, respectively. If the input signals to RF and LO ports are of the same frequency but with a phase difference ϕ, (5.2) can be rewritten as:

$$\text{Vout} = \frac{\pi}{2} g_m R_L \left[V_{RF} \cos(\phi) + V_{RF} \cos(2\omega_{RF} + 2\omega_{LO} + \phi) \right] \tag{5.3}$$

Filtering out the high frequency term by a LPF, one can further simplified (5.3) to be:

$$\text{Vout} = \frac{\pi}{2} g_m R_L V_{RF} \cos(\phi) = \frac{\pi}{2} g_m R_L V_{RF} \sin\left(\frac{\pi}{2} - \phi\right) \tag{5.4}$$

Figure 5.8 demonstrates the simulation results of a mixer cell designed with 0.18-μm CMOS model. The output voltage of the mixer is close to a real cosine wave with a small phase shifts $\Delta\phi$

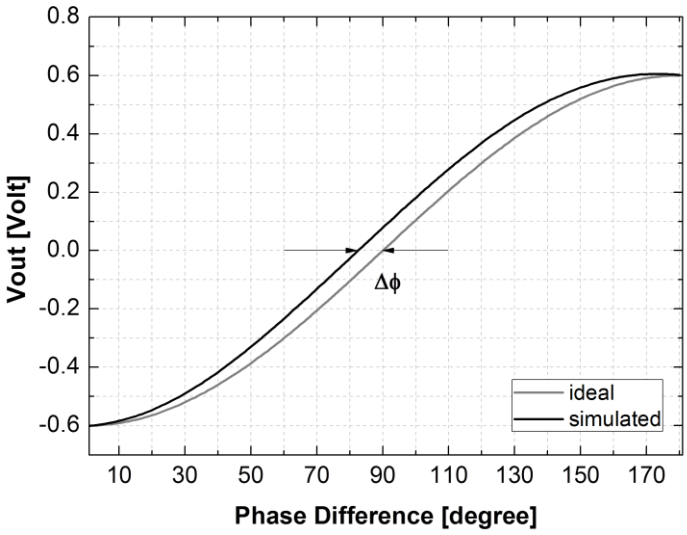


Figure 5.8 Simulated V_{out} vs. input phase difference, and a comparison with an ideal cosine function

resulting from the delay of the band-limited transistors in the mixer. The $\Delta\phi$, also known as the static phase offset, can be calculated as [68]:

$$\Delta\phi = \left(\tau_{tr,RF} \times f_{i,RF} + \tau_{tr,LO} \times f_{i,LO}\right) \times 360° \quad (5.5).$$

where $f_{i,RF}$ and $f_{i,LO}$ are the signal-frequency at the RF and LO inputs, respectively. In addition, $\tau_{tr,RF}$ and $\tau_{tr,LO}$ are the intrinsic channel transit time of transistors in RF ports and LO ports, respectively. They can be calculated based on the same equation:

$$\tau_{tr} = \frac{4}{3} \frac{\alpha L^2}{\mu_{eff}\left(V_{GS} - V_{TH}\right)} \quad (5.6),$$

in which α is a constant related to the body effect, μ_{eff} the effective mobility, L the channel length, V_{GS} the gate-to-source bias, and V_{TH} the threshold voltage of the transistor. For the case that a small $\Delta\phi$ is important, we could increase the overdrive voltage or reduce the channel length of the transistor in the mixer to get a smaller transit time which leads to a smaller $\Delta\phi$.

The cosine relation between the input and output only approximates a linear-in-degree relation at a small range of ϕ (when ϕ very close to $\pi/2$), and the slope of the curve is partly determined by the amplitude of input signal. These will generate phase control error if the PA in the predistortion operates in a back-off power, or if the phase distortion deviates too much from the original value. Therefore, the input signal to the RF ports, unlike the mixer design, should also pass through a limiting amplifier. The limiter should be able to saturate the input swing of the RF transistors for a wide range of the input power. The resulting mixer will then multiplying two square waves with the same frequency. Hence the output voltage will be much linearly related to the phase difference. Figure 5.9 shows the results from a simulation performed with the same Gilber cell, but with the RF and LO signals connected first to a limiting amplifier then to the mixer. The amplitude at the output of the limiting amplifier is 1.4 V_{PP}. Although the static offset becomes larger, the output curve of the mixer is now demonstrating a very good linear-in-degree relation. The phase error form the simulates curve to a fitted straight line, also known as

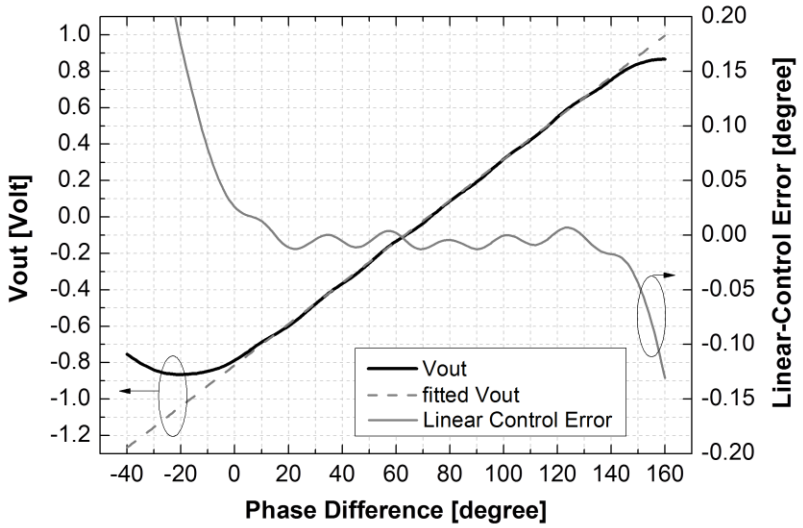


Figure 5.9 Simulated V_{out} vs. input phase difference and the linear-in-degree error

the linear-in-degree error, is less than ±0.05° for more than 140° phase range. The slope of this curve is now less relative to the input signal, and mainly determined by the g_m of the transistors. Inserting a phase shifter with small tunable range between V_{AM_OUT} and V_{PM_OUT} in Figure 5.1, a designer can easily cancels the effect of $\Delta\phi$, getting a zero voltage output when the phase difference is zero. The differential outputs of the phase detector are connected to an interfacing OP-Amp summing circuit similar to the one shown in Figure 5.6. The interfacing circuit adjusts the slope of the error curve, and adds a DC reference voltage to bias the VPS at zero phase shifts when the PA demonstrates no phase error.

5.3 LINEAR PA FOR MULTIBAND WCDMA UPLINK - AN EXAMPLE OF THE ANALOG PREDISTORTION SYSTEM

All the required circuit blocks for analog predistortion has been built in previous sections, the work left is to verify their functionality with a non-linear PA. This section demonstrates first the output from the AMED and the PMED that connected to a nonlinear PA, and the linearized results when the gain and phase controllers are activated. The nonlinear PA used to validate the functionality of the predistortion blocks is designed based on [65], but intentionally tuned to be less linear. The tuning is done through varying the transistor size, the LC values of the matching network, and the bias points by a small percentage from its original values (values that make PA work linearly). These variations are commonly observed in fabricated CMOS circuits because of the process variation.

Figure 5.10 shows the gain response of the nonlinear PA used in the system simulation. The

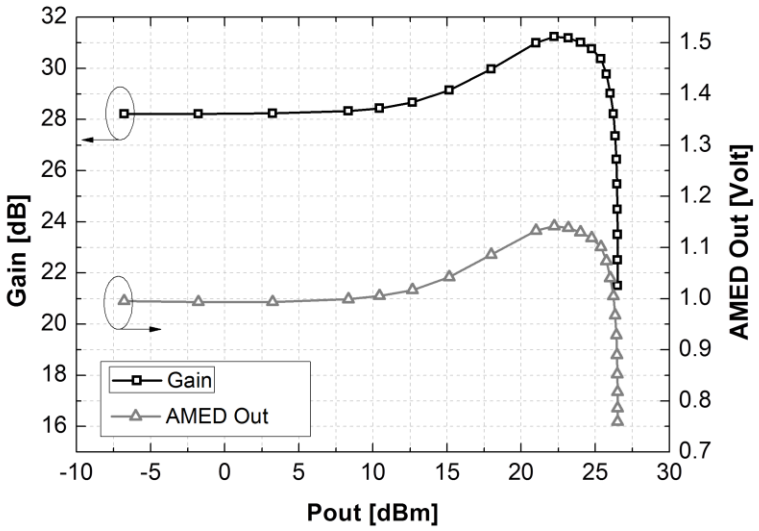


Figure 5.10 The Gain vs. Pout of a non-linear PA [65], and the output voltage of the AMED attached to the PA

gain peaking at a higher power is resulting from the gain expansion of the CS transistors in the PA. Gain expansion is a technique frequently used in designing a linear PA. The peaking should be less than 1-dB to reduce the AM/AM error; however, with a little variation of the design parameters, the peaking can easily exceeds 3-dB of the original gain. This gain peaking produces a non-unilateral gain variation, and requires an adaptive compensation.

On the other hand, the phase distortion produces by a gain-peaking PA, as shown in Figure 5.11, is not unilateral as well. The complicated PM error pattern cannot be eliminated by simply

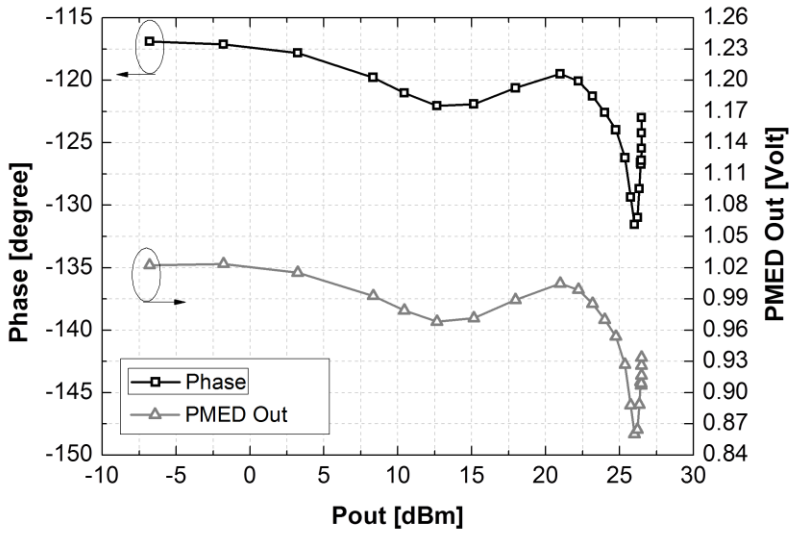


Figure 5.11 The Output Phase vs. Pout of a non-linear PA [65], and the output voltage of the PMED attached to the PA

putting a circuit that shows an increasing phase at higher input power. Again, an adaptive phase predistortion is required to linearize the phase response of such a nonlinear PA.

Before starting to compensate the PA, the functionality of the detection circuits needs to be verified. The aforementioned AM and PM error detectors are first connected to the input and output of the PA; their output voltages at different power level are as well plotted in Figures 5.10

and 5.11, respectively. In both figures, the outputs of the error detectors do track closely with the error, validating that they can be used to detect the gain and phase with minimum errors. By changing the resistance value in the interfacing analog adder in, the gain control curve of the predistorter can be easily matched to the error detector output, producing proper distortion to cancel the AM and PM errors of the non-linear PA.

5.3.1 AM/PM Error Correction of a Nonlinear PA

To predistort a non-linear PA, all the functional blocks are now connected as illustrated in Figure 5.1. A single tone simulation is run to validate the performance of the analog predistorter and the results are shown in Figures 5.12 to 5.15.

Figures 5.12 and 5.13 plot the amplitude related performance of the predistorted PA system. The gain peaking due to the gain expansion and variation of the design parameters is flattened by the gain control circuits. However, the maximum output power is still limited by the physical attribute of the transistors in the PA core, and the gain is clipped by the limitation.

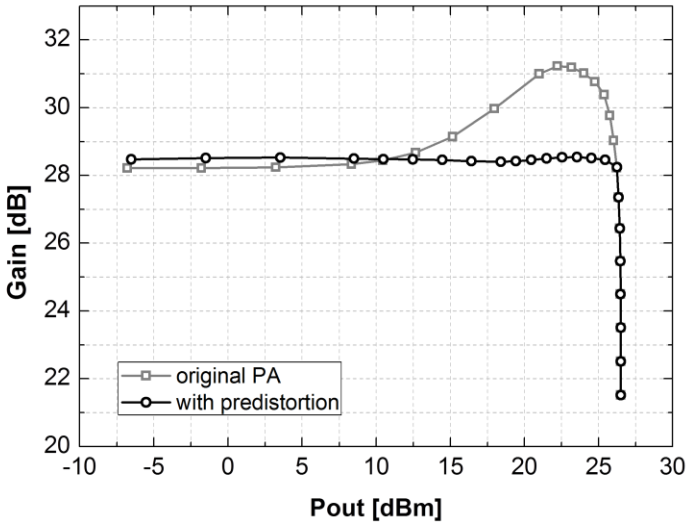


Figure 5.12 Gain vs. Pout of the non-linear PA with and without analog predistortion

Figure 5.13 shows the AM/AM errors of the predistorted PA. For an ideal linear PA, for any 1-dB increases in the input power, the output power should also increase by 1-dB. Hence the ideal AM/AM conversion should be 1 dB/dB. As the input power increases, a real PA cannot keep this relationship and starts to show some deviation. For the original non-linear PA used in

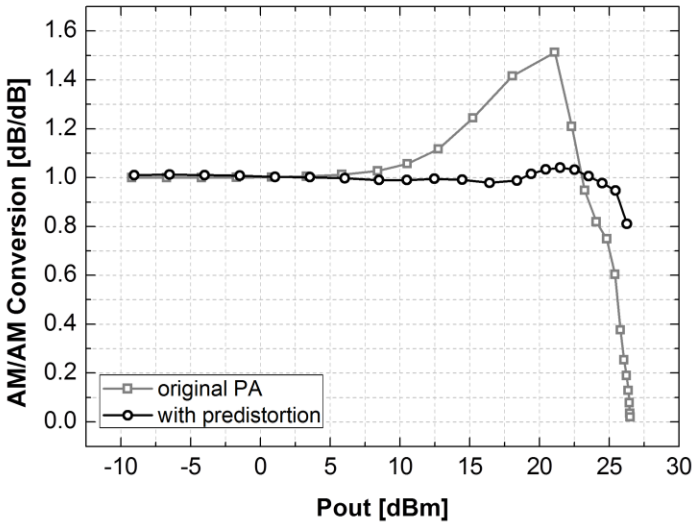


Figure 5.13 AM/AM Conversion of the non-linear PA with and without analog predistortion

the simulation, the AM/AM conversion has a maximum value of 1.5 dB/dB near the peak of the gain, and then drops quickly to 0.6 dB/dB. By applying the adaptive predistortion, the PA is able to keep its AM/AM conversion within 0.99 to 1.04 dB/dB for a wide range of input power. The VGA attached to the PA successfully reduces the AM/AM error from 50% to 4% before the PA reaches its saturation power.

On the other hand, the phase predistorter also demonstrates its ability for PM error cancellation. As shown in Figure 5.14, the phase response is flattened by the VPS attached in the input of the PA. The phase variation is reduced from 15° to 1.5° before the PA saturated at 27 dBm maximum output power. The AM/PM error is plotted in Figure 5.15. For an ideal linear PA,

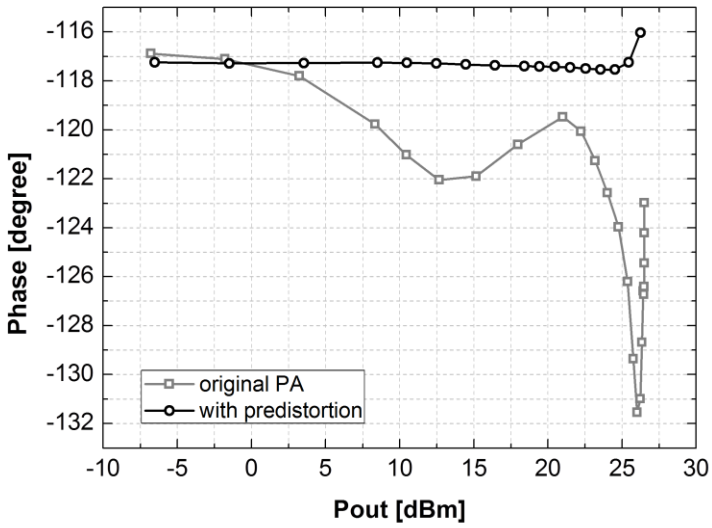


Figure 5.14 Gain vs. Pout of the non-linear PA with and without analog predistortion

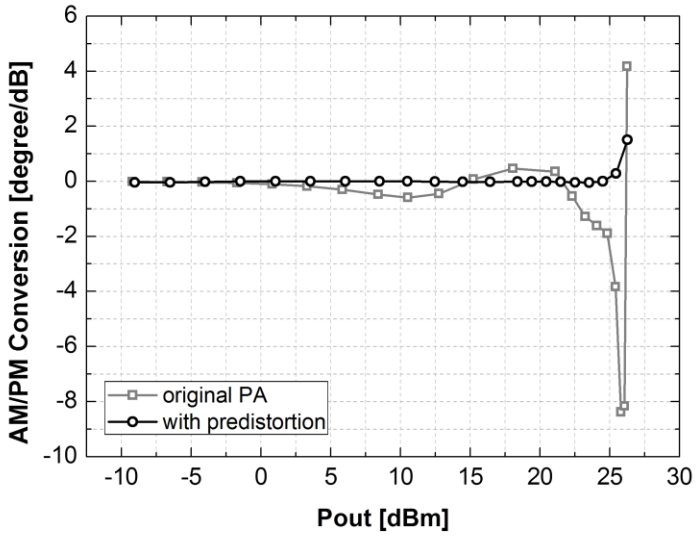


Figure 5.15 AM/PM Conversion of the non-linear PA with and without analog predistortion

the increase in input power should not affect the phase. Hence ideally the AM/PM conversion is 0 °/dB. For the non-linear PA used in this design, however, the AM/PM conversion changes from -8°/dB to 4°/dB. With the phase predistorter activated, this AM/PM conversion range is reduced to -0.03 °/dB to 0.3 °/dB.

In addition to the single tone simulation, the WCDMA modulated signals are also used to see the difference in performance between a PA with and without analog predistortion. The input WCDMA signals are centered at 1.95 GHz and have 3.84 MHz of bandwidth. The output power is around 26 dBm, which is 1-dB back-off from the saturated output power. Figure 5.16 shows output spectrum with referenced to the signal power at 1.95 GHz. The skirt of the PA with

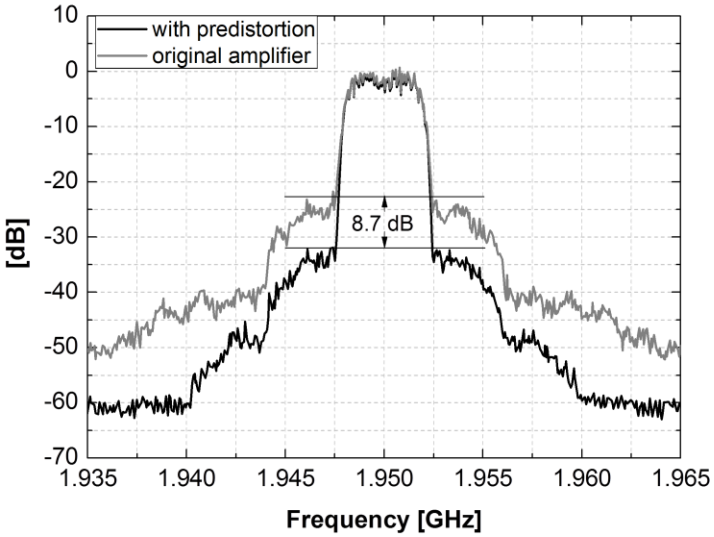


Figure 5.16 Output spectrum of a PA with and without analog predistortion. The simulation is performed with WCDMA modulated signal centered at 1.95 GHz, and the output power level is 26 dBm.

predistortion is obviously lowered. The ACPR of the PA at 5 MHz frequency offset is lowered by 8.7 dB, while the ACPR reduction is 12 dB at 10 MHz offset. In addition, the EVM value also improved from 5.9% to 2.4%. The total current consumed by the predistortion circuits is around 30 mA, and is drawn from a 1.8-V power supply (54 mW). The original PA consumes around 550 mA current from a 3.4-V supply (1.87 W) and has a peak power-added efficiency (PAE) around 40%. The extra power consumed by the predistortion circuits (includes the mixer, two logarithm amps and phase/gain controllers) will only reduce the PAE by around 1%. The

detailed comparison of the performance is summarized in Table 5.1. These clearly validate the functionality of the analog predistortion circuit.

Table 5.1 Summery of Simulated Results for the PA with and without predistortion

	Max. P_{OUT} [dBm]	**AM/AM* [dB/dB]**	**AM/PM* [°/dB]**	**ACPR (5MHz) [dBc]**	**ACPR (10MHz) [dBc]**	**EVM [%]**
Original PA	27	0.6 ~ 1.5	-8-4	26.78/26.81	42.04/41.92	5.979
w/ Predistortion	27	0.99~1.04	-0.03-0.3	35.34/35.59	58.63/58.55	2.413

*AM/AM and AM/PM values are the variation before the output power of the PA reaches 1-dB back-off of its maximum power

CHAPTER 6

CONCLUSIONS

6.1 SUMMARY OF THE RESEARCH

The research presented in this dissertation is about designing suitable functional blocks for analog predistortion PA in multi-standard wireless communication systems. It is motivated by a recent booming in the smart phone market and development in the advanced communication standards for wireless communications. Transferring data at a higher data rate has complicated the signal constellations and therefore the design of a transmitter, especially the PA. To implement a linear PA in CMOS technology, there must be circuits to compensate for the nonlinearity, namely, gain and phase distortion, originated from the physical characteristics of transistors in CMOS technology.

Chapter one briefly introduced several advanced modulation schemes for wireless communications and how they are related to the linearity issue of a transmitter. In addition, the chapter gives a brief introduction to the popular linearization techniques of power amplifiers in transmitters. After comparing the pros and cons of different linearization methods, the analog predistortion PA is chosen for its fast settling time and better stability. The later parts of the chapter then analyzed several conventional gain and phase pre-distortion circuits.

Chapter two presented a highly linear variable attenuator that can be used to predistort the amplitude of a signal with very high power. The design has been fabricated with a commercially

available 0.18-μm RF CMOS technology. A detailed analysis of different attenuator topologies shows that the proposed adaptive bootstrapped body biasing technique can effectively reduce variations in transistor impedance resulting from large input signals, thus improving the linearity of an attenuator. It also adds very limited complexity to the circuits, and is compatible with most of the conventional linearization techniques. It achieves a minimum IP_{1dB} and IIP_3 of 7.5 dBm and 17 dBm, respectively at 1.95 GHz. It also has a linear-in-dB attenuation control curve with an error less than ±1 dB over a 30 dB attenuation range. While overall S_{21} flatness from 400 MHz to 3.7 GHz is better than 2.6 dB, the worst-case input and output return losses are both better than -9 dB. The presented attenuator has the smallest size (750 × 375 μm^2), the best linearity performance, and the widest bandwidth among similar CMOS designs.

For those applications require less linearity but higher gain, a VGA topology optimized for linearity, bandwidth, and linear-in-dB controllability is presented in the chapter three. As compared to conventional VGA designs, this RF VGA topology is much suitable for implementing the amplitude pre-distorter in an analog-predistortion PA system. It utilizes a dynamically biased amplifier and a highly linear tunable attenuator to provide gain and linearity. The chapter also demonstrated that a self-biased differential pair can get the best use of a dynamic current boost for to compensate for gain reduction at a higher input power. Besides, the linearity-bandwidth tradeoff comes with different bootstrapped body bias resistances of the attenuator is analyzed. Finally, a RF VGA designed with such topology and targeted for wireless communication applications is fabricated in a commercial available standard 0.18-μm CMOS technology, and has an active area of 0.108 mm^2. The measurement results show that it has a linear-in-dB gain control curve from 380 MHz to 2.2 GHz with a maximum gain tuning range of 27 dB (13.5 dB to -13.5 dB) and less than ±1 dB error. Within this bandwidth, the flatness of

frequency response is less than 3 dB at every gain setting. The proposed RF VGA has a worst-case input P_{1dB} of -5 dBm and -3.6 dBm respectively at 850 MHz and 1950 MHz, while the minimum IIP_3 is 7.5 dBm at 1950 MHz. To our knowledge, this worst-case linearity performance is the best as compared to previous VGA works. Moreover, the post-attenuator structure gives this RF VGA a NF similar or even better to previous work when operating at a lower gain setting. The fabricated RF VGA consumes 11 mA from a 1.8-V power supply at DC and increases to 15 mA when the input power is 0 dBm.

In addition to the amplitude pre-distorter, the analog predistortion PA system requires a phase control circuit to compensate for the phase errors. Chapter four presented a novel poly-phase filter (PPF) and a gain control circuit that together give a vector-sum type variable phase shifter a compact size, a linear-in-degree control, and a small gain variation, while consuming a limited power. The proposed PPF topology reduces the number of stage required to generate a wideband I/Q split, thereby having a loss of 2-dB better than the traditional PPF design and giving the VPS a very small area ($0.063mm^2$) as compared to other CMOS works. The VPS has been fabricated in a commercial available 0.18-μm CMOS process. From the measurements, the control circuit of this VPS does keep the total current passing through the I and Q branches of the vector-sum amplifier a constant (2.3mA) over the phase control range. The constant current minimizes the gain variation at different phase shifts to around 1 dB. The control circuit also linearly relates the relative phase shifts to the input control voltages. The measured linear-in-degree error is ±1° within a phase control range of 70°, while the maximum phase variation range is 90°. The bandwidth of this phase shifter is from 1 GHz to 2 GHz. The gain flatness over this bandwidth is less than 3-dB while the phase control ranges are around 90°. This is able to cover most of the wireless communication uplink for mobile handsets.

With the gain and phase control circuits presented previously, it is able to build an analog predistortion PA system and verify the effectiveness of the predistorter. Chapter five introduces the remaining blocks in the system (an AM error detector designed with logarithm amplifiers and a PM error detector designed with a Gilbert cell mixer) and demonstrates the simulation results of the predistortion system. This includes a single tone and a WCDMA modulated signals (as an example of the advanced communication standards) test. The linearity characteristics are compared between a PA with and without predistortion. The proposed gain and phase control circuits are able to flatten both the gain and the phase of the PA at its saturated output power, and effectively reduce the ACLR, turning a PA that fails to meet the WCDMA requirements to one that pass all the linearity tests.

6.2 SUGGESTIONS FOR FUTURE WORK

The implementation for an analog predistortion PA system is not yet mature. Although the dissertation has demonstrated the ability of CMOS circuits in controlling the gain and phase under a larger input power, the other critical blocks like accurate amplitude detection and phase detection circuits remain challenging.

An accurate amplitude detection circuits is easy to implement with CMOS models and with only simulation. However, non-ideal effects such as DC offset problem, parasitic effects from layout structure, and power supply variation due to PA will deviate the voltage vs. input power curve from the simulated value. Besides, in order to match the amplitude of signal sampled at the input and the signal sampled at the output, extra attenuators has to be put in the detection path. After the circuits are fabricated, all the non-ideal effects may require the designer to fine-tune the

bias or gain of each individual blocks. The yield issue resulted from a requirement for accurate amplitude control will prevent the circuits from the mass production.

Similarly, implementing an accurate phase detection circuits are still very challenging in CMOS technology. Again, the phase variation due to parasitic effects necessitates extra tunable phase control circuits been put in the detection path to calibrate the phase control curve. Besides, because the output of the mixer-type phase detector not only depends on the phase but also on the amplitude of the input signal. Therefore, an mixer based phase detector needs a high gain limiter to achieve better accuracy. The limiters should generate small phase distortion even when its output voltage swing is saturated. If a PA that has 26 dB to 30 dB of gain starts to produce phase error at 10 dBm output power, the limiter connected to the input port will be handling an input signal with a power around -16 to -20 dBm. The limiter then has to magnify the signal to around 1-V_{PP}, so that the phase detector will have a better phase resolution (a large input voltage swing for the mixer input gives the output better phase detection resolution). Such a limiter operates in the RF domain will both consume a very high DC current and need inductive loads to peak its gain, increasing the overall PA size and degrading its efficiency dramatically.

Therefore, the traditional linear-in-dB or linear-in-degree detection circuits may be unsuitable for the implementation of an analog predistortion PA system. To implement a realistic and commercially-competitive analog predistortion PA system, researchers in both academia and industry must devoted further efforts in both inventing new circuit topologies for gain and phase detection circuits, as well as for circuits serving as the interface between the control and detection blocks that helps create a perfect error cancellation.

REFERENCES

[1] C. D. Presti, F. Carrara, A. Scuderi, P. M. Asbeck, and G. Palmisano, "A 25 dBm digitally modulated CMOS power amplifier for WCDMA/EDGE/OFDM with adaptive digital predistortion and efficient power control" *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1883–1896, Jul. 2009.

[2] W. Woo and J. S. Kenney, "A predistortion linearization system for high power amplifiers with low frequency envelope memory effects," *IEEE MTT-S Dig*., May 2005, pp. 1545-1548.

[3] B. Razavi, *RF Microelectronics* Englewood Cliffs, NJ: Prentice-Hall, 1998.

[4] *S*J. K. Cavers, "Adaptation Behavior of a Feedforward Amplifier Linearizer," *IEEE Trans. Veh. Technol.*, vol. 44, no. 1, pp. 31-40, Feb. 1995.

[5] S. Narahashi and T. Nojima, "Extremely Low-Distortion Multi-Carrier Amplifier-Self-Adjusting Feed-Forward (SAFF) Amplifier," in *Proc. IEEE Int. Conf. Commun.*, vol. 3, June 1991, pp. 1485-1490.

[6] M. G. Choi, Y. C. Jeong, and I. H. Park, "*Method and Apparatus for Amplifying Feedforward Linear Power Using Pilot Tone Hopping*," US Patent No. 6,081,156, 2000.

[7] R. H. Bauman, "*Adaptive Feedforward System*," US Patent No. 4,389,618, 1983. Y. Yang, Y. Kim, J. Yi, J. Nam, B. Kim, W. Kang, and S. Kim, "Digital Controlled Adaptive Feedforward Amplifier for IMT-2000 Band," in *IEEE MTT-S Int. Microwave Symp. Dig*., vol. 3, June 2000, pp. 1487-1490.

[8] M. G. Overmann and J. F. Long, "*Feedforward Distortion Minimization Circuit*," US Patent No. 5,077,532, 1991.

[9] D. Fisher and D. Dobkin, "A temperature-compensated linearizing technique for MMIC attenuators utilizing GaAs MESFETs as voltage-variable resistors," in *IEEE MTT-S Dig.*, May 1990, pp.781–784.

[10] Y. Araki, T. Hashimoto, and S. Otaka, “A 0.13μm CMOS 90dB variable gain pre-power amplifier using robust linear-in-dB attenuator,” *IEEE RFIC. Symp. Dig.*, Jun. 2008, pp. 673–676,.

[11] H. Dogan, R. G. Meyer, and A. M. Niknejad, “Analysis and design of RF CMOS attenuators,” *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2269–2283, Oct. 2008.

[12] H. Kondoh, “DC-50 GHz MMIC variable attenuator with a 30 dB dynamic range,” in *IEEE MTT-S Dig.*, Jun. 1988, pp. 499–502.

[13] B. Maoz, “A novel, linear voltage vartiable MMIC attenuator,” *IEEE Microw. Theory Tech.*, vol. 38, no. 11, pp 1675-1683, Nov. 1990

[14] Miyatsuji, K., Ueda, D., “A low-distortion GaAs variable attenuator IC for digital mobile communication system,” *IEEE Proc. of ISSCC*, Buena Vista, USA, Feb. 1995, pp.42-43.

[15] H. D. Lee, K. A. Lee, S. H. Hong, “A wideband CMOS variable gain amplifier with an exponential gain control,” *IEEE Microw. Theory Tech.*, vol. 5, no. 6, pp 1363-1373, Jun. 2007

[16] H. Elwan, A. Tekin, and K. Pedrotti, “A Differential-Ramp Based 65 dB-Linear VGA Technique in 65 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2503–2514, Sep. 2009.

[17] R. Harjani, “A low-power CMOS VGA for 50-Mb/s disk drive read channels,” *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 42, no. 6, pp. 370–376, Jun. 1995.

[18] W. M. Christopher, “A variable gain CMOS amplifier with exponential gain control,” in *VLSI Circuits Tech. Dig. Symp.*, Jun. 2000, pp. 146–149.

[19] P. Huang, L. Y. Chiou, and C. K.Wang, “A 3.3-V CMOS wideband exponential control variable-gain-amplifier,” in *Proc. IEEE Int. Circuits Syst. Symp.*, May 1998, pp. I-285–I-288.

[20] Y.-S. Youn, C.-S. Kim, N.-S. Kim, and H.-K. Yu, “A 1 GHz-band low distortion up-converter with a linear in dB control VGA for digital TV tuner,” in *IEEE Radio Freq. Integrated Circuits Symp. Dig.*,May 2001, pp. 257–260.

[21] Y.-S. Youn, J.-H. Choi, M.-H. Cho, S.-H. Han, and M.-Y. Park, "A CMOS IF transceiver with 90 dB linear control VGA for IMT-2000 application," in *VLSI Circuits Tech. Symp. Dig.*, Jun. 2003, pp. 131–134.

[22] C. T. Fu, and H. Luong, "A CMOS linear-in-dB high-linearity variable gain amplifier for UWB receivers," in *Proc. IEEE ASSCC'07*, pp. 103–106.

[23] J. Xiao, I. Mehr, and J. Silva-Martinez, "A high dynamic range CMOS variable gain amplifier for mobile DTV tuner," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 292–301, Sep. 2007.

[24] H. Zarei, S. Kodama, C. T. Charles, and D. J. Allstot, "Reflective-type phase shifters for multiple-antenna transceivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 8, pp. 1647–1656, Aug. 2007.

[25] Y. Zheng, C. E. Saavedra, "An ultra-compact CMOS variable phase shifter for 2.4 GHz ISM applications," *IEEE Tran. Microw. Theory and Tech.*, vol. 56, no. 6, pp. 1349-1354, Jun. 2008

[26] R. Kaunisto, P. Korpi, J. Kiraly, and K. Halonen, "A linear-control wideband CMOS attenuator," in Proc. *IEEE ISCAS 2001*, Sydney, Australia, 2001, vol. 4, pp. 458–461.

[27] H. Dogan and R. G. Meyer, "Intermodulation distortion in CMOS attenuators and switches," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 529–539, Mar. 2007.

[28] M. T. Terrovitis and R. G. Meyer, "Intermodulation distortion in current-communicating CMOS mixers," *IEEE J. Solid-State Circuits,* vol. 35, no. 10, pp 1461-1473, Oct. 2000.

[29] Y. Tsividis, K. Suyama, and K. Vavelidis, "Simple reconciliation MOSFET model valid in all regions," *Electron. Lett.*, pp506-508, Mar 1995.

[30] M. Ahn, C.H. Lee, B.-S. Kim, and J. Laskar, "A high-power CMOS switch using a novel adaptive voltage swing distribution method in multistack FETs," *IEEE Trans. Microw. Theory Tech*, vol. 56, no. 4, pp. 849–858, April. 2008.

[31] M. Ahn, H.W. Kim, C.H. Lee, and J. Laskar, "A 1.8-GHz 33-dBm P0.1dB CMOS T/R switch using stacked FETs with feed-forward capacitors in a floated well structure," *IEEE Trans. Microw. Theory Tech*, vol. 57, no. 11, pp. 2661–2670, Nov. 2009.

[32] B.-W. Min and G. M. Rebeiz, “A 10-59-GHz CMOS distributed step attenuator with low loss and low phase imbalance,” *IEEE J. Solid-State Circuits,* vol. 42, no. 11, pp 2547-2554, Nov. 2007.

[33] L. Boglione and R. Pavio, “Temperature and process insensitive circuit design of a voltage variable attenuator IC for cellular band applications,” *IEEE Microwave and Guided Wave Letters*, Vol. 10, No. 7, pp.279 – 281, July 2000.

[34] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K. Y. Lin, Y.-T. Chang, and H.Wang, “Design and analysis for a miniature CMOS SPDT switch usingbody-floating technique to improve power performance,” *IEEE Trans. Microw. Theory Tech*, vol. 54, no. 1, pp. 31–39, Jan. 2006.

[35] R. G. Meyer and P. R. Gray, Analysis and Design of Analog Integrated Circuits, 4th ed. New York: Wiley, 2001.

[36] B. Razavi, Design of Analog CMOS Integrated Circuits. Boston, MA: McGraw-Hill, 2001.

[37] V. W. Leung, L. E. Larson, P. S. Gudem, “Digital-IF WCDMA handset transmitter IC in 0.25-μm SiGe BiCMOS,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2215–2225, Dec. 2004

[38] Y.-Y. Huang, W. Woo, C.-H. Lee, and J. Laskar, “A CMOS wide-bandwidth high-power linear-in-dB variable attenuator using body voltage distribution method,” *IEEE RFIC Symp. Dig.*, May. 2010, pp. 673–676

[39] Y.-Y. Huang, W. Woo, Y, Yoon, and C.-H. Lee, “Highly linear RF CMOS variable attenuators with adaptive body biasing,” paper accepted to *IEEE J. Solid-State Circuits*

[40] K. Han, L. Zou, Y. Liao, H. Min, and Z. Tang, “A wideband CMOS variable gain low noise amplifier based on single-to-differential stage for TV tuner applications,” *IEEE Asian. Solid-State Circuits Conf. Dig.*, Nov. 2008, pp. 457–560

[41] D. Im, H.-Kim, and K. Lee, “A CMOS resistive feedback differential low-noise amplifier with enhanced loop gain for digital TV tuner applications,” *IEEE Tran. Microw. Theory Tech.*, vol. 57, no. 11, pp 2633-2462, Nov. 2009

[42] M. Meghdadi, M. S.-Bakhtiar, and A. Medi, “A UHF variable gain amplifier for direct-conversion DVB-H receivers,” *IEEE RFIC Symp. Dig.*, May. 2009, pp. 551–554

[43] S. M. Taleie, Y. Han, T. Copani, and B. Bakkaloglu, S. Kiaei, “A 0.18μm CMOS fully integrated RFDAC and VGA for WCDMA transmitters,” *IEEE RFIC Symp. Dig.*, Jun. 2008, pp. 157–160

[44] S.-F. Chang, W.-L. Chen and C.-H. Hsu, “CMOS dual-band variable-gain amplifier for 3G-WCDMA and WLAN dual-mode RF receivers,” *IEE Electronic Letters*, vol. 43, issue 2, pp. 102-103, Jan. 2007

[45] C.-H. Wu, C.-S. Liu, and S.-I. Liu, “A 2GHz CMOS variable-gain amplifier with 50dB linear-in-magnitude controlled gain range for 10GBase-LX4 Ethernet,” *IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2004, pp. 484–541

[46] Z. Li, F. Guo, D. Chen, H. Li, and Z. Wang, “A wideband CMOS variable gain amplifier with a novel linear-in-dB gain control structure,” *IEEE Intl. RFIT workshop Dig*, Dec. 2007, pp. 337-340

[47] H. Akyol, B. Agarwal, H. A. Firouzkouhi1, and D. A. Badillo, “A CMOS dB-linear RF VGA for SAW-less WEDGE transmitters,” *IEEE RWS Dig.*, Jan. 2010, pp. 57–60

[48] C.-C. Huang and W.-C. Lin, “Compact high-efficiency CMOS power amplifier with built-in linearizer,” *IEEE Microw. and Wireless Components Lett.,* vol. 19, no. 9, pp. 587-589, Sep. 2009

[49] D. Chowdhury, C. D. Hull, and O. B. Dega “A fully integrated dual-mode highly linear 2.4 GHz CMOS power amplifier for 4G WiMax applications,” *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3393–3402, Dec. 2009

[50] K.-S. Lee, H. Jeon, Y. Yoon, H. Kim, J. Kim, and C.-H. Lee, “A linearity improvement technique for a class-AB CMOS power amplifier with a direct feedback path,” *IEEE Asian. Solid-State Circuits Conf. Dig.*, Nov. 2010, pp. 1–4

[51] K.-J. Koh and G. M. Rebeiz, “0.13-m CMOS phase shifters for X-, Ku-, and K-band phased arrays,” *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535-2546, Nov. 2007

[52] M. J. Gingell, “Single sideband modulation using sequence asymmetric polyphase networks,” *Electr. Commun.*, vol. 48, no. 1 and 2, pp. 21–25, 1973.

[53] J. Kaukovuori, K. Stadius, J. Ryynänen, and K. A. I. Halonen,“Analysis and design of passive polyphase filters,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 10, pp. 3023–3037, Nov. 2008.

[54] C. Lu, A. V. Pham, and D. Livezey, “Development of multiband phase shifters in 180-nm RF CMOS technology with active loss compensation,” *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 40–45, Jan.2006.

[55] D. R. Banbury, N. Fayyaz, S. Safavi-Naeini, and S. Nikneshan, “A CMOS 5.5/2.4 GHz dual-band smart-antenna transceiver with a novel RF dual-band phase shifter for WLAN 802.11a/b/g,” in IEEE Radio Freq. Integr. Circuits Symp., Fort Worth, TX, Jun. 2004, pp. 157–160.

[56] M. Meghdadi, M. Azizi, M. Kiani, A. Medi, and M. Atarodi,”A 6-bit CMOS phase shifter for S-band,” *IEEE Tran. Microw. Theory and Tech.*, vol. 58, no. 12, pp. 3519-3526, Dec. 2010

[57] Y. Zheng and C. E. Saavedra, “Full 360 vector-sum phase-shifter for microwave system applications,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 4, pp.752-758, Apr. 2010

[58] J.-C. Wu, T.-Y. Chin, S.-F. Chang, and C.-C. Chang, “2.45-GHz reflection-type phase shifter MMICs with minimal loss variation over quadrants of phase-shit range,” *IEEE Tran. Microw. Theory and Tech*., vol. 56, no. 10, pp. 1349-1354, Oct. 2008

[59] H. Zarei and D. J. Allstot, “A low-loss phase shifter in 180 nm CMOS for multiple-antenna receivers,” in *IEEE Int. Solid-State Circuits Conf.*,San Francisco, CA, Feb. 2004, pp. 392–534.

[60] M. A. Y. Abdalla,K. Phang, and G. V. Eleftheriades, “Printed and integrated CMOS positive/negative refractive-index phase shifters using tunable active inductors,” *IEEE Tran. Microw. Theory and Tech*., vol. 55, no. 8, pp. 1611-1623, Aug. 2007

[61] G. Zhang, S. Khesbak, A. Agarwal, and S. Chin, “Evolution of RFIC handset PAs,” *IEEE Microw. Magzine*, Feb. 10, pp. 60-69.

[62] F.Wang, D. F. Kimball, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelopetracking OFDM power amplifier," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1271–1281, Jun. 2007.

[63] V. Pinon, F. Hasbani, A. Giry, D. Pache, and C. Garnier, "A singlechip WCDMA envelope reconstruction LDMOS PA with 130 MHz switched-mode power supply," in *IEEE Int. Solid-State Circuits Conf. Tech*. Dig., pp. 564–56, Feb. 2008.

[64] J. Choi, D. Kim, D. Kang, B., Kim, "A polar transmitter with cmos programmable hysterestic-controlled hybrid switching supply modulator for multistandard applications," *IEEE Tran. Microw. Theory and Tec*h., vol. 57, no. 7, pp. 1675-1686, Jul. 2009.

[65] H. Jeon, K.-S. Lee, O. Lee, K. H. An, Y. Yoon, H. Kim, D. H. Lee, J. Lee, C.-H. Lee, and J. Laskar, "A 40% PAE linear CMOS power amplifier with feedback bias technique for WCDMA applications," *IEEE RFIC. Symp. Dig.,* pp. 561-564, Jun. 2010.

[66] P.-C. Huang, Y.-H. Chen ,and C.-K. Wang, "A 2-V 10.7MHz CMOS limiting amplifier/RSSI," *IEEE J. Solid-State Circuits*, vol. 35 no. 10, pp. 1474-1480, Oct. 2000

[67] W.L. Barber and E.R. Brown, "A true logarithmic amplifier for radar IF applications," *IEEE J. Solid-State Circuits*, vol. 15 no. 13, pp. 291-295, Mar. 1980

[68] J. Carr and B. Frank, "Static phase offset in a multiplying phase detector," *IEEE Microw. and Wireless Components Lett.,* vol. 19, no. 9, pp. 518-520, Sep. 2009

PUBLICATIONS

[1] **Y.-Y. Huang**, W. Woo, Y. Yoon, C.-H. Lee, and J. Laskar, "Highly linear RF CMOS variable attenuators with adaptive body biasing," *IEEE J. Solid-State Circuits*, vol. 46 , pp. 1023-1033 , May 2011

[2] **Y.-Y. Huang**, W. Woo, C.-H. Lee, and J. Laskar, "A CMOS wide-bandwidth high-power linear-in-dB variable attenuator using body voltage distribution method," in *IEEE Radio Freq. Integr. Circuits Symp.*, June 2010, pp. 303-306

[3] **Y.-Y. Huang**, W. Woo, H. Jeon, C.-H. Lee, and J. S. Kenney, "A compact wideband linear CMOS variable gain amplifier for analog-predistortion power amplifiers," paper submitted to *IEEE Tran. Microw. Theory and Tech*

[4] **Y.-Y. Huang**, H. Jeon, Y. Yoon, W. Woo, C.-H. Lee, and J. S. Kenney, "An ultra-compact, linearly-controlled variable phase shifter designed with a novel RC poly-phase filter," paper submitted to *IEEE Tran. Microw. Theory and Tech*

[5] H. Jeon, Y. Park, **Y.-Y. Huang**, J. Kim, K.-S. Lee, C.-H. Lee, and J. S. Kenney, "A triple-mode balanced linear CMOS power amplifier using switched quadrature coupler," *IEEE International Solid-State Circuits Conference (ISSCC)*, Student Research Forum, Feb 2011

VITA

Yan-Yu Huang was born in Taipei, Taiwan, in 1984. He received the B.S. degree in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan in 2006, and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, in 2009. Since 2007, he has been working toward the Ph.D. degree in electrical and computer engineering at Georgia Institute of Technology.

His major research interests includes Analog/RF tunable circuits design, such as variable attenuators, variable gain amplifiers and phase shifters using bulk CMOS process.